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Influence of parameters inherent to ohmic contacts on properties of microwave avalanche transit-time diodes

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Abstract. In this paper, a review of microwave avalanche transit-time diode (IMPATT diode) structures has been presented. The structure of IMPATT diode with a sharp *p-n* junction on Si has been considered, and functions of the ohmic contacts have been shown. Physical and technical requirements for contacts have been formulated as based on their functional purpose and the existing technological base. A review of existing ohmic contacts and their ranking in terms of suitability and promising use in IMPATT diode have been made. The structure of metallization for IMPATT diode was chosen in the framework of the specificity of the IMPATT diode operation.

Keywords: avalanche transit-time diode, ohmic contact, annealing temperature, current transfer mechanism.

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1. Introduction

The development of semiconductor microwave electronics requires an increase in the output power of solid-state microwave-wave generators. Modern avalanche transit time diodes (IMPATT diode) operate in this frequency range of output power of the order of ≥10 W in the pulsed mode. To achieve such initial parameters, there arises the need to use stable ohmic contact with multilayer metallization with the specific contact resistance of the order of $\rho_c \le 10^{-5}$ Ohm·cm^2. An important factor for the use of high-power pulsed IMPATT diode in microwave circuits is account of the specific features of the thermal mode of the diode. To avoid overheating the diode in the pulsed mode, it is necessary to take into account the influence of the specific contact resistance not only on the output parameters, but also on the heating of the semiconductor part of the diode. When developing an ohmic contact, one should take into account the specifics of its use in a specific semiconductor device and its influence on the main parameters of the device, on the basis of which the requirements for the contact are formulated. Usually, it is not possible to create ohmic contact, a resistance of which is much smaller than that of the base area, the temperature dependence of the specific contact resistance affects the temperature dependence of the IMPATT diode output parameters, generation frequency and power. Therefore, one of the important requirements for the ohmic contact to IMPATT diode is a weak temperature dependence.

2. The principle of action of the avalanche transit-time diode

Operation of avalanche transit-time diodes is based on the appearance of a negative differential resistance (NDR) region in voltage-current characteristic (VCC) of the inversely shifted *p-n* junction at the breakdown section, when a certain value of current exceeds the critical one [1, 2]. The negative differential resistance is associated with that voltage and current are in the opposite phase in a certain period of time. The delay in the avalanche increase in the amount of carriers is manifested by the final time of the avalanche current rise, and the delay in passage of an avalanche through the semiconductor structure – due to the final time of carrier passage in the drift region. NDR appears at such a frequency that the sum of these time intervals is equal to the half-period of oscillation. On the inverse VCC, one can observe a downward area, which is called the area with a negative differential resistance.

The paper [3] shows possible types of IMPATT diode. Therefore, as a model, the silicon biavalanche transit-time diode with homogeneous doping the avalanche areas was taken.

3. Influence of ohmic contacts on the output characteristics of avalanche transit-time diodes. Physical and technical requirements to contacts for silicon subTHz IMPATT diode

When developing the ohmic contact, it is necessary to take into account specificity of its use in a particular semiconductor device and its influence on the basic parameters of the device, on the basis of which the requirements for contact are formulated. Let us consider the basic requirements for ohmic contact for IMPATT diode. Let's consider the distribution of heat along the structure of IMPATT diode (Fig. 1). The heat flux is mainly generated in the band of *p-n* junction and is removed through the lower ohmic contact into a massive heat sink.

The main parameter of IMPATT diode is the maximum generation power at the optimal frequency P_{out}, which depends on the applied power P_{in} and efficiency η that weakly grows with increasing the temperature T [4]:

$$P_{\text{out}} = P_{\text{in}}\eta(T). \tag{1}$$

The maximum operation power that can be applied to the IMPATT diode P_{in} is determined using the formula:

$$P_{\text{in}} = \left(T_{j\,\max} - T_{\text{case}}\right) \Big/ R_{th\ jc}(1-\eta), \tag{2}$$

where T_{case} is the body temperature; $R_{th\,jc}$. – thermal resistance of the *p-n* junction body; $T_{j\,\max}$ – maximum operation temperature on the *p-n* junction, at which the set operation time up to failure is provided. This temperature may be limited by the temperature of degradation of the ohmic contact [5].

The thermoelectrophysical processes in the *p-n* junction can also limit the operation temperature of the *p-n* junction. Operation of IMPATT diode in the constant mode was modeled up to the temperature 277 °C [6], and it was shown that the efficiency of IMPATT diode increases before 227 °C, but with increasing the temperature to 277 °C the efficiency begins to fall sharply.

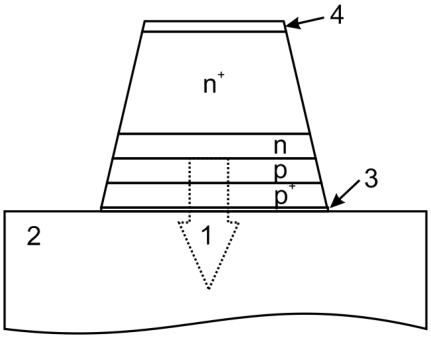

Fig. 1. Typical IMPATT DIODE design.

For silicon impulse IMPATT diode, it is usually recommended the limit operation temperature of the *p-n* junction is not higher than 250 °C at a generator temperature of 50 °C. Also, for the pulsed mode, operation of IMPATT diode is recommended at 350 °C [7], which indicates the possibility of operation at this temperature also in the constant mode under condition of stable ohmic contact. It allows maximizing the output power of the device, despite the decrease in efficiency. It is worth noting that the temperature of the resistance to overheating (which may occur, for example, when soldering the device, impulse overloads) and the maximum operation temperature differ considerably. To evaluate the required resistance temperature of the ohmic contact to overheating one can use the known dependence between the temperature and average operating time to failure in silicon: with a decrease in temperature by 40 degrees, the average operation time to failure increases by an order of magnitude. That is, without even considering other mechanisms of degradation, in order to provide 10,000 hours of the operation time to failure, the temperature of contact stability during rapid thermal annealing must be higher than the maximum operation temperature by ΔT_{Ar} = 230 degrees. That is, in order to the ohmic contact does not limit the maximum parameters of the silicon IMPATT diode in the constant mode of operation, it must be resistant to rapid thermal annealing at the temperature $T_{\max}$ = 250 °C + + 230 °C = 480 °C. Although the upper contact is under more unfavorable temperature conditions, however, less stringent conditions regarding the thickness of the junction are placed to it as compared to the lower contact, which in our case makes it possible to form contact through a simplified procedure without degrading the IMPATT diode parameters. In order to clarify the temperature of degradation of the lower ohmic contact, it is necessary to take into account the temperature drop on the semiconductor thickness.

Since the main source of heat release is the *p-n* junction region, then the thermal resistance consists of the thermal resistance of *p-p*$^+$ sections and the thermal resistance spreading in copper. Contributions from the thermal spreading resistance in copper heat sink in $R_{th\,\text{Cu}}$ and in *p-p*$^+$ sections ($R_{th\,\text{Cu}}$) are related to the size and are calculated by the formula:

$$R_{th} = R_{th\ \text{Si}} + R_{th\ \text{Cu}} = \left(\frac{h_2}{\lambda_{\text{Si}}} + \frac{r}{\lambda_{\text{Cu}}}\right) \Big/ S, \tag{3}$$

where S is the area of the diode mesastructure, λ_{Si}, λ_{Cu} are the coefficients of thermal conductivity of silicon and copper, respectively, λ_{Si} = 0.8 W/cm·deg, λ_{Cu} = = 3.9 W/cm·deg; r – radius of the diode mesastructure; the thickness of the *p-p*$^+$ areas h_2 = 1.5 μm. For comparison, $R_{th\,\text{Si}}$ = 0.41 deg/W; $R_{th\,\text{Cu}}$ = 6.8 deg/W. When using not copper, but diamond heat sink $R_{th\,\text{diamond}}$ = 2.6 deg/W. Accordingly, the temperature at the ohmic

contact T_{con} will be lower than that in the *p-n* junction area and equals:

$$T_{\text{con}} = T_{\text{case}} + P_{\text{in}}(1-\eta)R_{th\ \text{Cu}}. \quad (4)$$

At the temperature near the *p-n* junction $T_{j\ \max} = 250$ °C, the temperature at the ohmic contact will be:

$$T_{\text{con}} = T_{\text{case}} + \left(T_{j\ \max} - T_{\text{case}}\right)\frac{R_{th\ \text{Cu}}}{R_{th\ \text{Si}} + R_{th\ \text{Cu}}}. \quad (5)$$

In regard to a copper heat sink, $T_{\text{con}} = 236$ °C, for a diamond one $T_{\text{con}} = 217$ °C. The required maximum temperature of rapid thermal annealing without degradation of the contact will be:

$$T_{\max\ Cu} = T_{case} + \left(T_{j\ \max} - T_{\text{case}}\right)\frac{R_{th\,\text{Cu}}}{R_{th\,\text{Si}} + R_{th\,\text{Cu}}} + \Delta T_{\text{Ar}}. \quad (6)$$

The required maximum temperatures of the rapid thermal annealing without degradation of the contact for the lower ohmic contact will be

$T_{\max\ \text{Cu}} = 236$ °C + 230 °C = 466 °C;

$T_{\max\ \text{diamond}} = 217$ °C + 230 °C = 447 °C.

That is, in both cases the maximum power is limited by the temperature of the degradation of the ohmic contact.

Of course, this estimate does not take into account the geometric factor. For example, the conicity of the structure leads to a some decrease in the thermal resistance of the p^+-layer, limited by the length of the heat sink. A more radical way to reduce thermal resistance is multi-mesa compositions. Calculation of the thermal resistance of a multi-mesa compositions is listed, for example, in [7], where, due to multi-mesa composition at a frequency of 60 GHz, the output of continuous power at the level of 1 W is reached, which corresponds to the modern level of output power of IMPATT diode with diamond heat sink. However, such a construction introduces additional inductance in series, which may limit its use with frequency growth.

The requirement for the highest possible temperature stability of contacts to the rapid thermal annealing is not the only requirement for them. An important technological parameter is the thickness of the junction area. Under the thickness of the junction area, we will understand the depth of penetration of the contact material into the bulk of semiconductor during the forming annealing, as well as the defects caused by this process. The value of the junction area of the ohmic contact should be much less than the thickness of the high-doping layer (p^+-area), in order to prevent contamination of the drift area with the contact material and germination of defects into the active area. On the other hand, an increase in the thickness of the p^+-area causes not only an increase in the active electric resistance, but also an increase in the thermal resistance (see formula (3)), which reduces the maximum output power.

Therefore, ideally, the thickness of the p^+-area should be much smaller than the thickness of the *p*-area. The thickness of the *p*-area falls with the frequency [8]: for IMPATT diode at 95 GHz – 0.3…0.38 μm, at 220 GHz – 0.16 μm, *i.e.*, it is desirable to limit the thickness of *p*-area with the value of 0.2 to 0.12 μm, respectively. On the other hand, requirement of a thin junction layer is limited by the requirement of good adhesion, that is, the interpenetration of the materials of contact and semiconductor should provide their good mechanical adhesion, which will not degrade under the influence of mechanical stresses that will arise during operation due to the difference in the coefficients of thermal expansion for the materials of contact and semiconductor.

These considerations concern only the lower ohmic contact, to the upper contact such strict conditions are not placed. However, for technological reasons, metallization of the upper contact should not increase the amount of materials needed to form the contacts, that is, it consists of the same layers contained in the lower contact.

Consider also the requirements for the specific resistance of ohmic contacts to IMPATT diode. With an increase in the resistance in series R_s that is the sum of the resistance in series of the diode base and the contact resistance $R_s = R_{ss} + R_c$, the negative differential conductivity G becomes closer to zero [9]:

$$\frac{G}{G_m} = \frac{3 + 2R_sG_m - \sqrt{(3+2R_sG_m)^2 - 16R_s\left(G_m + 2R_s\omega^2C^2\right)}}{8R_sG_m}, \quad (7)$$

where G_m is the idealized negative differential conductivity, provided $R_s = 0$, ω – cyclic frequency, C – capacitance. Let introduce the substitution $\alpha = -G_mR_s$ and quality factor $Q = -\frac{\omega C}{G_m}$ [10]. The quality factor Q gives information about the threshold and the rate of oscillation growth when IMPATT diode is used for generation.

$$\beta(\alpha, Q) \equiv G_m^{-1}G = \frac{3}{8\alpha} - \frac{3}{8}\sqrt{\frac{1}{\alpha^2} - \frac{4}{9}\frac{1}{\alpha} + \frac{4}{9} - \frac{32}{9}Q^2} + \frac{2}{8}. \quad (8)$$

When $R_s = 0$, the variable α is converted to 0, the efficiency is maximal. When R_s grows to the limit where α converts to 1, the efficiency decreases to 0. When G_m is constant, $G \propto 1/R_s$

Then, the drop of the efficiency (relative to some ideal efficiency at $R_s = 0$) depends on the resistance in series as follows:

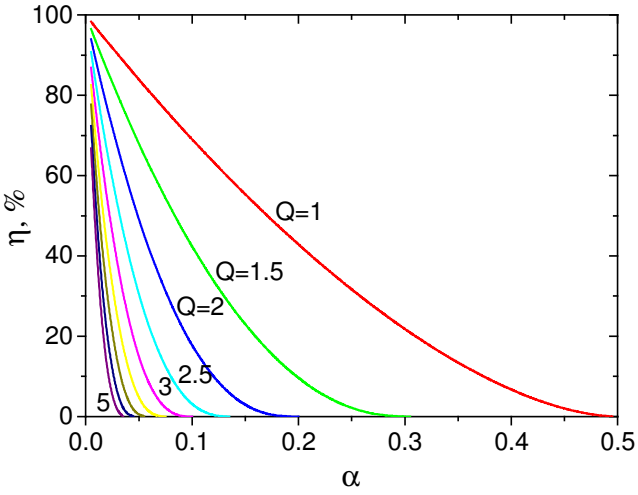

Fig. 2. Dependence of the efficiency on α.

$$\eta_t = \frac{P}{P_{\max}} = \frac{27}{4G_m}\left(1-\frac{G}{G_m}\right)^2\left(G - R_s G^2 - R_s \omega^2 C^2\right). \qquad (9)$$

We get the efficiency as a function of two variables – α and Q:

$$\eta_t = \frac{27}{4}(1-\beta)^2\left(\beta + \alpha\beta^2 + \alpha Q^2\right). \qquad (10)$$

Characteristic Q-values for silicon biavalanche TTD at 95…98 GHz are equal to 3.3…3.8, and the resistance in series of base reaches $(6.7\ldots8.7)\cdot10^{-6}$ Ohm·cm^2 [11]. As you can see from Fig. 2, in order to minimize the effect of the ohmic contact on the characteristics of IMPATT diode, the specific resistance of the contact should be much less than the resistance in series of base caused by other factors. Technological expedient of formation of the p^+-area in the conical form somewhat reduces the requirements to contact [11], since increases its area in comparison with the area of the p-n junction. However, in terms of contact resistance and in terms of thermal resistance, their contribution is limited to the length of spreading. Take, for example, the concentration in the p^+-area 10^{20} cm^{-3}. In this case, the length of transfer will be

$$L_t = \sqrt{\frac{\rho_c h}{\rho_s}}, \qquad (11)$$

where ρ_s is the specific resistivity of semiconductor in the p^+-area, h – thickness of the p^+-area.

At the thickness $h = 2\cdot10^{-5}$ cm, the specific resistance 10^{-3} Ohm·cm, and the specific contact resistance $\rho_s = 10^{-6}$ Ohm·cm^2, the gain to the radius is about 1.4 μm, which will give a gain in the area at the diameter 35 μm no more than 17%.

Since it is usually not possible to create an ohmic contact, which resistance would be neglected in comparison with the resistance of base area, the temperature dependence of the specific contact resistance influences the temperature dependence of the initial parameters of IMPATT diode, generation frequency and power. Therefore, one of the important requirements for ohmic contact to LPD is a weak temperature dependence.

The main feature in operation of active microwave elements based on IMPATT diode is that the mode of microwave generation is quite sensitive to the presence of hetero-geneity of various origin: dislocations, aggregations of structural defects both in the operation layer and in the metal-semiconductor contact. The active part of the diode is actually located in the near-surface layer of semiconductor, and even a small dispersion of structural properties (for example, near-surface microstresses) is sufficient enough that the IMPATT diode parameters are substantially deviated from the calculated ones or ultrahigh-frequency generation did not occur at all. Therefore, else one important parameter of ohmic contact is the level of internal mechanical stresses, boundary defectness and defectness at the metal-semiconductor interface.

4. Requirements for ohmic contacts in IMPATT diode

Being based on the abovementioned, we formulated the requirements for the ohmic contact, the fulfillment of which is necessary for its successful use in silicon IMPATT diode in the ultrahigh-frequency range:

- specific contact resistance is not higher than 10^{-6} Ohm·cm^2;
- weak temperature dependence of the specific contact resistance;
- temperature stability is not worse than up to 350 °C [5] (optimally to 466 °C);
- contact should also be stable to the influence of other degradation factors that may occur during its operation (radiation and ultrasound radiation, thermal cycling);
- metal-semiconductor contact boundary (<100 nm) that is thick and homogeneous in morphology and phase composition;
- good adhesion;
- minimization of internal mechanical stresses at the metal-semiconductor interface;
- the processes of formation of a contact must be compatible with the technological scheme of formation of the device itself.

To obtain recommendations for creating the optimal contact in silicon IMPATT diode, a review of the literature data on the properties of the formed ohmic contacts to silicon was made, which is given below.

5. Modern level of ohmic contact technology

One of the main parameters of ohmic contacts is the value of resistivity. The minimum value of the specific resistance depends on the current flow mechanism through the metal-semiconductor structure. Through the ideal metal-semiconductor contact, the following current flow mechanisms are possible [12, 13]:

1. Thermoelectric current flow mechanism.
2. Thermal field mechanism of current flow.
3. Field mechanism of current flow.
4. Current flow in metal shunts.

This approach allows us to determine the dominant current flow mechanism at the temperature T.

Figs 3 and 4 show the results of using different types of metallization to form an ohmic contact in the system of dependence of the specific contact resistance ρ_c on the concentration of both donor (N_d) and acceptor (N_a) impurities. The solid line indicates the minimum contact resistance calculated with account of the three above-mentioned current flow mechanisms. The dashed line indicates the maximum permissible resistance of ohmic contacts for IMPATT diode in the millimeter wavelength range. Further, we will consider only contacts with the values of the contact resistance below this line, *i.e.*, with the specific resistance not higher than 10^{-6} Ohm·cm^2.

Previously, we can see that only ohmic contacts to the highly doped silicon satisfy the requirement of minimum contact resistance, which makes the presence of n-n^+ and p-p^+ steps in the design of the IMPATT diode mandatory. As shown in Figs 3 and 4, the above requirement satisfies the contacts on the basis of metals: platinum, aluminum, zirconium, vanadium, tungsten; silicides: of titanium, platinum, nickel, cobalt. Deposition of finished silicides often gives preference in the thickness of the interface of the annealed contact.

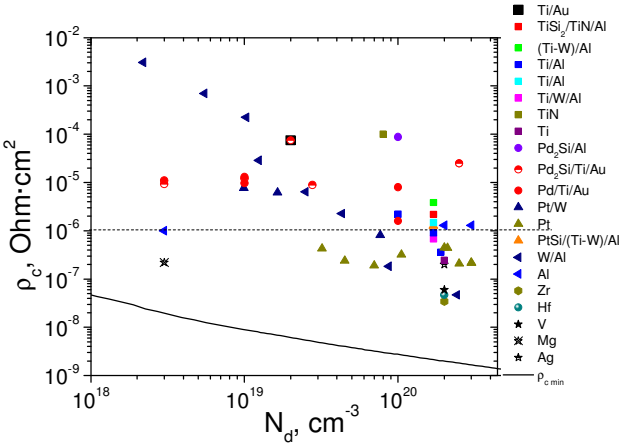

Fig. 3. Results of the use of metallization to form the ohmic contact in the system to plot the dependence of the specific contact resistance ρ_c on the concentration of donor impurity (N_d) [14-29].

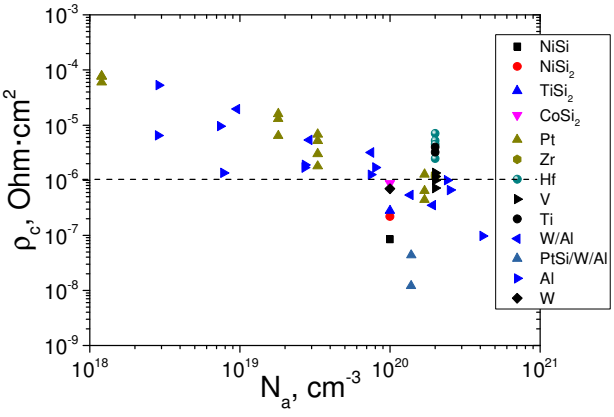

Fig. 4. The results of using metallization to form an ohmic contact in the system to plot the dependence of the specific resistance ρ_c on the concentration of acceptor impurity (N_a) [20, 26, 29, 30, 32-39].

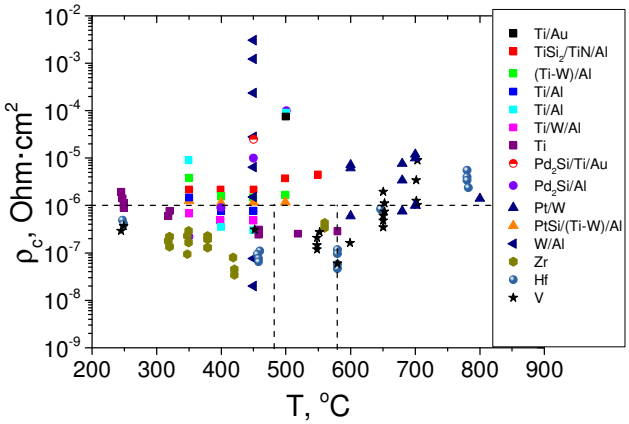

Fig. 5. The dependence of the specific contact resistance (ρ_c) on the annealing temperature (T) of the silicon n-Si ohmic contacts [20, 24, 27, 31, 34-39].

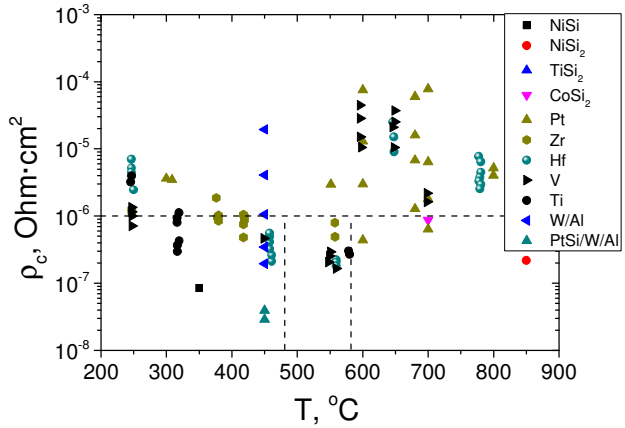

Fig. 6. The dependence of the specific contact resistance (ρ_c) on the annealing temperature (T) of the silicon p-Si ohmic contacts [20, 31, 34, 35].

When forming the ohmic contact to semiconductor, the following concepts and their combinations are generally used.

First, it is possible to select the work function in contact materials, so that, for *n*-type semiconductor, the work function of electrons from metal or compound that was formed during the annealing, φ_m, must be less than that from semiconductor, φ_s, and between metal and *p*-type semiconductor $q\varphi_m > q\varphi_s$. However, this relation is true provided when the junction layer is absent, and the density of surface states at the interface is relatively low. At high levels of surface density, the Fermi level is fixed, and the barrier height is weakly dependent on $q\varphi_m$, which corresponds to the Bardeen limit. The density of surface states can be largely changed by the technological treatment of a semiconductor plate before and after deposition of an ohmic contact. In other words, the set of technological conditions for preparation of the semiconductor surface, methods of deposition and parameters of annealing, to a large extent, can define the specific resistance of the contact.

Secondly, extreme doping of a thin surface layer of semiconductor to provide conditions for tunneling current. These contacts do not require, at least in theory, thermal annealing. However, in practice, most of them are subjected to additional annealing to achieve a minimum value of contact resistance and maximum temperature stability. Another way of obtaining the doped surface layers is to dope the surface from an external source of doping impurity. Doping can also be achieved by ion implantation of the corresponding types, but it leads to the following problems: increased defectness of the near-surface layer and loss of stoichiometry.

Technology of manufacturing ohmic contact, as a rule, is a set of compromise solutions between adhesion and diffusion permeability of the anti-diffusion layer, between the value of the contact resistance and thickness of the junction layer, temperature stability and others. [38, 39]. Depending on the purpose of the contact and the requirements for its parameters, it can consist of one or more layers having different functional values.

In all the above-mentioned current flow mechanisms, to achieve a low value of the specific contact resistance is possible by reducing the height of the potential barrier at the interface of the contact-forming layer/semiconductor.

Technology of diffusion ohmic contact consists of formation of thin strongly doped n^+- and p^+-layers (steps of doping) at the contact-semiconductor interface. They are usually formed during diffusion or ionic doping of the near-contact area of semiconductor with further metallization.

In Figs. 5 and 6, in the system of dependence of the specific contact resistance from the annealing temperature, the results of formation of ohmic contacts with different levels of doping of *n*- and *p*-type silicon, respectively, are shown. It is evident that as contact-forming layer the following refractory materials – V, Hf, Zr, Ti, W, PtSi, WSi – satisfy the requirements of resistivity and heat resistance.

6. Conclusions

From the analysis of literature data and our calculated ones, we can draw the following conclusions:

1. Due to well-developed technology, silicon ultrahigh-frequency IMPATT diodes in the range 80 to 400 GHz are currently the leaders in output power among solid-state small-size generators.

2. A further increase in the power and frequency generation of IMPATT diode puts new demands to ohmic contacts. On the basis of the analysis of literary data and own calculations, a model of the influence of the ohmic contact parameters on the output power of IMPATT diode: the maximum temperature of rapid thermal annealing (formulae (1) to (6)), the thickness of the junction layer and $p^+(n^+)$ area as an addition to the thermal resistance (formulae (1)–(3)), the specific contact resistance and resistance of $p^+(n^+)$ area as an addition to the basis active resistance (formulae (1), (10)).

3. The technical requirements to ohmic contacts for IMPATT diode of the ultrahigh-frequency range have been formulated, the review of the literature data on the formed contacts has been performed.

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