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Effect of different parameters on the carrier mobility in NWTFET

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Abstract. In this paper, we have studied the effect of different parameters on carrier mobility in NWFET devices. Their characteristics have been investigated using the non-equilibrium Green function (NEGF) method. Our work involves the carrier mobility μ as a function of V_{DS} taken from 0.1 V to 1 V for various gate lengths, namely: 10, 20, 30, 40, and 50 nm. Then, the variation of μ as a function of width of the nanowire varied from 2 up to 6 nm. After that, we have simulated μ as a function of the oxide thickness for the values: 2, 4 and 6 nm. Moreover, the mobility has been considered as dependent on the composition of high-*k* materials, namely: SiO_2, HfO_2, ZrO_2. Our results clearly show that device characteristics can be improved by selecting geometrical and physical parameters.

Keywords: nanotransistor, NWFET, mobility, NEGF.

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1. Introduction

Within the next five to ten years, the semiconductor industry will face the greatest challenge in its history. The conventional planar bulk MOSFETs will reach their physical and technical limits and continuation of Moore's law will depend on novel and original device structures. We approach two challenges with the development of next generation nanotransistors such as the ability of modeling reasonable extended structures on an atomistic basis and prognostic simulation that are faster and cheaper. Modelling and simulation of semiconductor devices provides an important method of analysis; easily verified, communicated and understood [1–5]. Before any fabrication can be carried out, there is a need to simulate so as to improve understanding, save costs and time. More importantly, it can also predict unknown future behaviors of devices and define ways of reaching such lofty ideals. The theme of semiconductor technology is to scale down the size of transistor and to increase integration of transistor in a single chip. Advanced semiconductor devices have been scaled down to nanometer level and the device sizes are continually shrunk as predicted. Semiconductor nanomaterials have been an important research topic, due to properties distinct from those of bulk materials [6–8].

2. NWFET structure

A nanowire field-effect transistor (NWFET) is an electronic device that can act as a normal transistor (Fig. 1). As such, it has a channel which consists of a nanowire through which electrons can flow from the source to the drain contacts. A coaxial gate electrode, separated from the channel by an oxide layer, controls the current value. The geometry of NWFET can be seen in the following picture.

The NWFETs using a semiconducting nanowire generally have a metal-semiconductor-metal (MSM) structure. The metal-semiconductor (MS) contacts can be classified as Schottky and ohmic contacts. Most NWFETs are composed of two Schottky contacts connected back to back in series with a semiconducting nanowire operating as an intrinsic NWFET. The intrinsic NWFET model will include the current conduction of bulk charges through the center neutral region and of

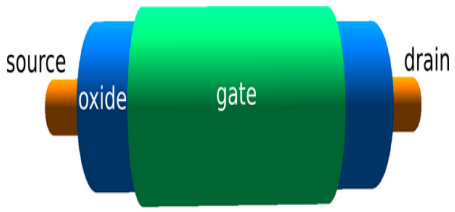

Fig. 1. Nanowire field effect transistor (NWFET) considered in this study.

accumulation charges through the surface accumulation region. Thus, it will include all current conduction mechanisms of NWFET operating at various bias conditions.

3. Drain-source current

To simulate the device proposed, a self-consistent solution of the Poisson and Schrödinger equations have been performed within the non-equilibrium Green function (NEGF) formalism with a mode space approach presented in [9, 10]. The NEGF method is an ideal approach for nanoscale device simulations where the device is characterized by an active region connected to two reservoirs. When one applies an external bias between the source and drain, the current drives the system into the non-equilibrium state, the NEGF approach is used to calculate the density matrix from which all other quantities of interest, such as current, can be obtained [11]. The Poisson equation gives the electrostatic potential needed for calculating the Hamiltonian of the carbon nanotubes (CNT). By solving the Schrödinger equation with the NEGF method, the density of states and the charge on the surface of CNT is obtained. The new electrostatic potential is obtained through the use of the calculated charge and solving the Poisson equation. We note that the ballistic transport is assumed here. It is convenient to solve Poisson's equations in cylindrical coordinates. Since the potential and charge are invariant around the nanotube, the Poisson equation can be written as [12, 13]:

$$\nabla \cdot \varepsilon \nabla \Psi(r) = -q\left(p - n + N_d^+ + N_a^-\right), \tag{1}$$

where Ψ is the potential of vacuum level, ε is the material permitivity, q – electric charge, n – electron density, p – hole density, N_d^+ – concentration of donor ions, and N_a^- – concentration of acceptor ions.

Schrödinger's equation is given by the expression:

$$H\Psi(x,y,z) = E\Psi(x,y,z), \tag{2}$$

$$H = -\frac{\hbar^2}{2m_x^*(x,y)}\frac{\partial^2}{\partial x^2} - \frac{\hbar^2}{2m_y^*(y,z)}\frac{\partial^2}{\partial y^2} - \\ -\frac{\hbar^2}{2m_z^*(x,z)}\frac{\partial^2}{\partial z^2} + U(x,y,z), \tag{3}$$

where H is the device Hamiltonian, m_y^* and m_z^* are the electron effective masses. The electron and hole concentrations (n and p, respectively) are computed by solving the Schrödinger equation with open boundary conditions by means of the NEGF formalism.

$$\nabla \cdot J_n = q \cdot R_n + q \cdot \frac{\partial n}{\partial t}, \tag{4}$$

$$\nabla \cdot J_p = -q \cdot R_p + q \cdot \frac{\partial p}{\partial t}, \tag{5}$$

$$J_n = q \cdot \mu_n \left(-n\nabla v + \frac{k_B T}{q} \cdot \nabla n\right), \tag{6}$$

$$J_p = q \cdot \mu_p \left(-p\nabla v + \frac{k_B T}{q} \cdot \nabla p\right), \tag{7}$$

where $J_{n,p}$ is the carrier current density. R_n, R_p are the net electron-hole pair recombination rate, k_B is the Boltzmann constant. The electron density is computed from the density of states (DOS), derived by the NEGF formalism. It can be calculated as follows:

$$n = \int_{E_i}^{+\infty} \left[D_S f\left(E - E_{FS}\right) + D_D f\left(E - E_{FD}\right)\right] dE, \tag{8}$$

where E_i is the Fermi level within the nanowire, $f(E)$ – Fermi-Dirac distribution, and $D_S(D_D)$, $E_{FS}(E_{FD})$ are the densities of states and the Fermi energies of the source (drain), respectively. A similar expression can be applied for holes. The source-drain current can be expressed as:

$$I = \frac{4q}{h}\int T(E)\left[f\left(E - E_{FS}\right) - f\left(E - E_{FD}\right)\right] dE, \tag{9}$$

where h is Planck's constant and $T(E)$ is the transmission coefficient calculated using the NEGF formalism [14].

4. Simulation analysis and results

The source and drain extension are homogeneously doped. The channel is assumed to be intrinsic. In this section, we present the results obtained from the simulation that is related to the influence of gate length, nanowire width, oxide thickness, gate dielectric permittivity and drain voltage V_{DS} on the carrier mobility μ behavior.

Fig. 2 illustrates the variation of I_{DS} as a function of drain voltage for different values of the gate length. Indeed, the mobility decreases when the gate length increases, the highest value is reached for L_g = 10 nm at V_{DS} = 0.8 V, which agrees with Fig. 3 that shows the importance of channel length in NWFET. A higher carrier mobility is achieved by having a shorter channel length. The latter also causes a higher mobility of electrons, which leads to a better performance especially for high speed devices.

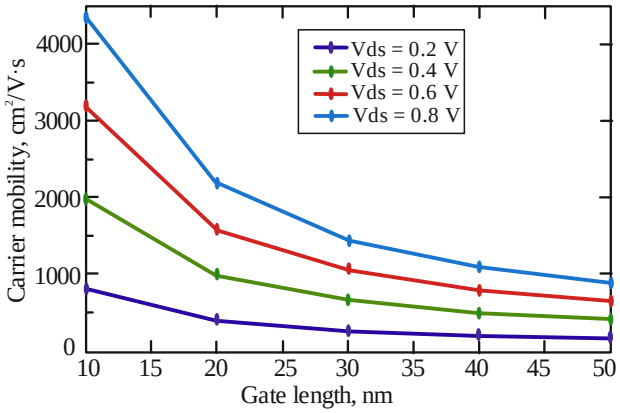

Fig. 2. Carrier mobility *versus* the gate length for different values of V_{DS}.

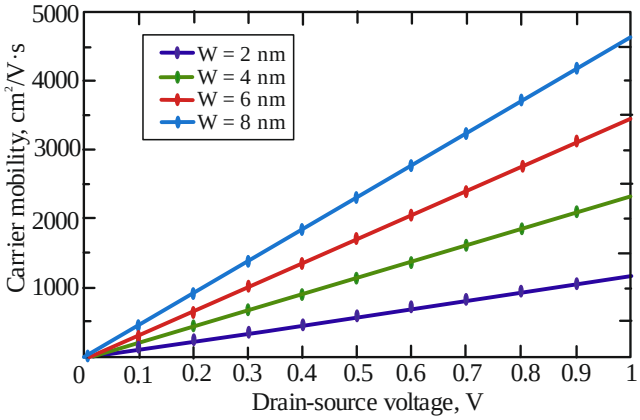

Fig. 5. Carrier mobility *versus* the drain source voltage for different values of nanowire width *W*.

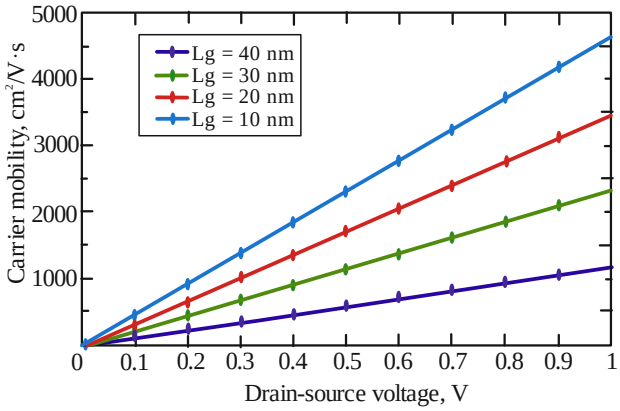

Fig. 3. Carrier mobility *versus* the drain-source voltage for different values of the gate length L_g.

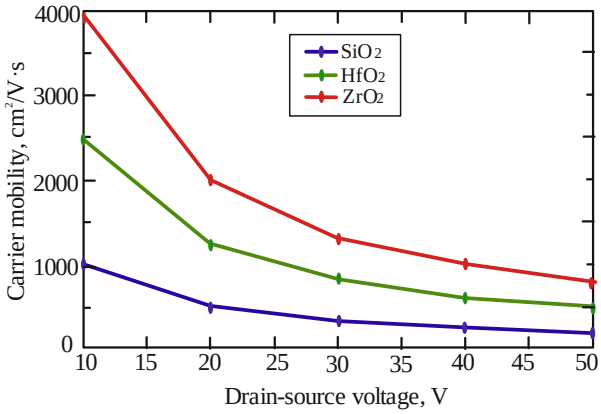

Fig. 6. Carrier mobility *versus* the gate length for different values of high-*k* materials, namely: SiO_2, HfO_2 and ZrO_2.

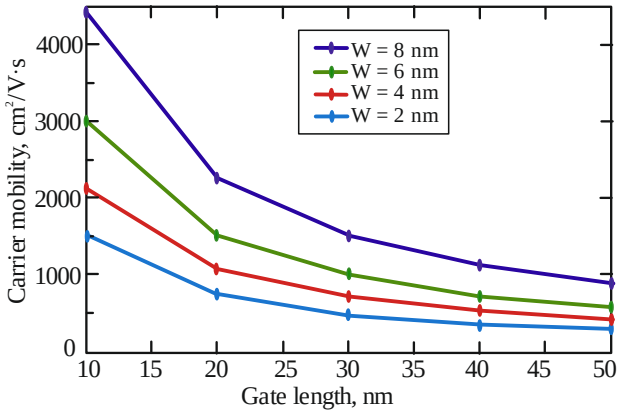

Fig. 4. Carrier mobility *versus* the gate length for different values of nanowire width *W*.

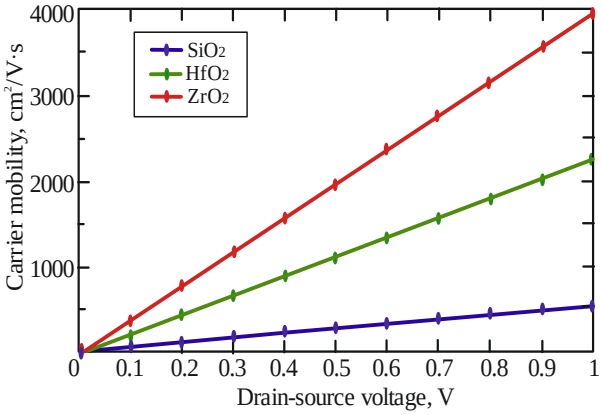

Fig. 7. Carrier mobility *versus* the drain-source voltage for different values of high-*k* materials, namely: SiO_2, HfO_2, ZrO_2.

On the other hand, we also noticed the carrier mobility μ corresponding to the nanowire ($W = 6$ nm, $L_g = 10$ nm) is higher than that obtained from the nanowire having ($W = 2$ nm, $L_g = 10$ nm) (Fig. 4). The best μ performances were observed for the largest widths (see Fig. 5).

Fig. 6 shows the mobility μ as a function of the gate length for three different gate oxides having three different dielectric permittivity k_{ox}. We chose for these three dielectric materials the following *k*-values: $k_{ZrO2} = 40$, $k_{HfO2} = 22$ and $k_{SiO2} = 3.9$. Simulations have shown that the carrier mobility μ

is higher for higher dielectric permittivity and shorter gate length as in Fig. 7 that shows how the carrier mobility increases with the *k*-value of these dielectrics. The use of a high-*k* gate dielectric is to overcome the gate leakage due to high direct tunneling of electrons through the oxide and reduce circuit power dissipation.

We have studied the effect of scaling oxide thickness t_{ox} on the performance of nanowire field effect transistor NWFET. It has been observed that reduction in the oxide thickness causes conductivity. Also, it can be concluded that when the oxide thickness is reduced, the carrier mobility and the current of the device increase (Fig. 8), but the leakage current I_{off} decreases. It can be considered as improvement over the most emerging carbon nanotubes and conventional MOSFETs, where the leakage current remains constant. It is further concluded that the switching speed of the device increases with reduction in the oxide thickness. Thus, the less oxide thickness is better option for enhancing the performance of NWFET (Fig. 9).

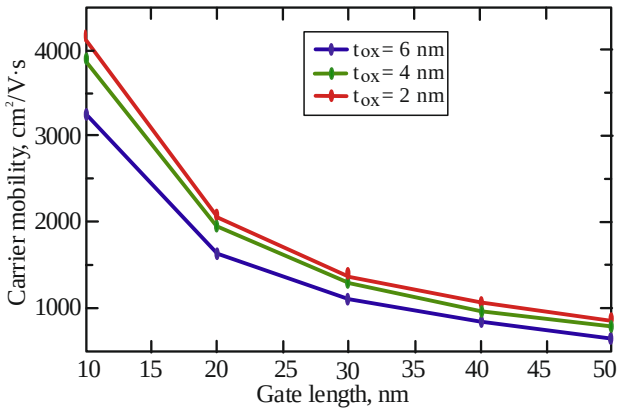

Fig. 8. Carrier mobility *versus* the gate length for different values of the oxide thickness t_{ox}.

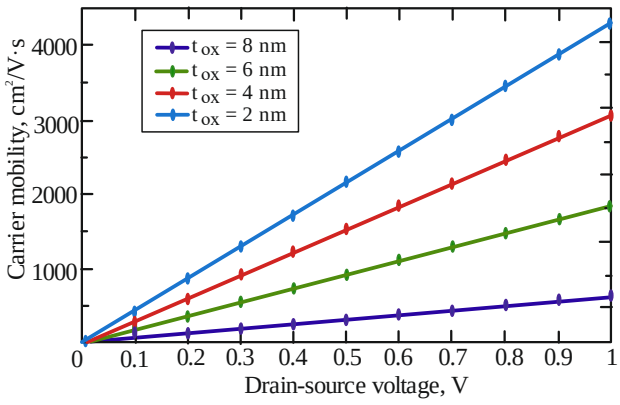

Fig. 9. Carrier mobility *versus* the drain-source voltage for different values of the oxide thickness t_{ox}.

5. Conclusions

In this study, we investigated the impact of different parameters on the carrier mobility of NWTFET in the nano-scale regime by using the non-equilibrium Green function (NEGF) formalism. The key settings of nanotransistors: gate length, nanowire width, oxide thickness and gate dielectric permittivity were studied. It has been found that the nanowire width has a direct impact on the transport properties, and the best performances were observed for the largest nanowire width. Also, we have observed a direct effect of the gate oxide thickness and dielectric constant on the carrier mobility characteristics. The mobility was found to be larger for the thinnest oxide layer and highest dielectric permittivity. Finally, the mobility was found to be significantly improved by reducing the gate length.

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