Optoelectronics and optoelectronic devices

New thermal small-signal model for FP-HEMT used in satellite communication application

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Abstract. In this paper, we study a field plate high electron mobility transistor (FP-HEMT) device with Al_2O_3 passivation, InAlN/GaN lattice matched, and a gate of 30-nm length. We simulate its performances evaluation in function of the thermal effect mode. We also show the analysis and simulation of this device with the proposed equivalent circuit that consists of inter-electrode distributed extrinsic parasitic and additional intrinsic feedback. Then, a study on how it can be used in thermal environment for satellite application. The simulator Tcad-Silvaco software has been used to predict results of the characteristics specified with a genetic algorithm, to improve the computation time and model accuracy. The obtained results confirm the feasibility of using this new device model with InAlN thin barrier, Filip Chip and field plate at the same time and in one structure at high power amplifier signal mode, as well as in a geostationary thermal orbital.

Keywords: HEMT, thermal effect, telecom satellite, power amplification.

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1. Introduction

In the geostationary satellites particularly, the thermal management is absolutely critical for maintaining the required thermal conditions in high power communication components [1].

The requirement of the design, development and implementation of passive and active thermal management with the higher capacity and power is growing in space applications exponentially. Hence, thermal management is very critical and of utmost importance for new devices in this domain.

In satellite advanced systems, the strong radiation is a major challenge. Thus, new structured devices that have special features which take care of high bandwidth capacity and high speed data communications such as Ku bands are very highly required. Though, high thermal conductivity materials can be a useful tool for that future devices design, which invites us to lurking out on it in this paper. Gallium nitride (GaN)-based microelectronics are of the most exciting semiconductor technologies for high power density and high frequency in the power electronics. Nevertheless, the very high power density in the active region of GaN HEMTs leads to a significant degradation in performance, particularly with the continuous increase of the device temperature [2].

The future thermal space application based on optimized III-N materials with HEMT devices technology have successfully achieved various advantage [3]. That leads to InAlN which is an excellent candidate for high temperature applications of wide band-gap semiconductors; it has many features, mostly the high breakdown field and the thermal activation, especially with the introduction of lattice matched InAlN/GaN [4, 5]. Moreover, AlN also possesses high spontaneous polarization in materials matrix, and a Curie temperature well above 1000 °C [6]. SiC is considered as the best substrate, it has minimum temperature variation along the electrode width [7]. New technologies present a wide range of challenges in the design of standard device, layout generation and validation of correct function.

Thus, the development of new tools being able to deal with these challenges is mandatory. This work presents a HEMT device placement in space environment technic by using simulation associated to analytical programming. The thermal model and update methods are used to reduce the search space environment of possible solutions, while analytical equations are used to find out the position of each that device in the layout.

2. Schematic and modeling of device circuit

Among the various types of power amplifiers in the context of telecommunication satellites application, the HEMTs with high power have emerged. The role of the designer is to find a way to operate a device in power thermal mode, and provide it with more energy in the new layout, which making it possible to exploit the best its potentialities and its performances (high power, high frequency, high sheet carrier density, low on-resistance value and channel-operating in very high temperature), and benefit this advantage as maximum possible as makes this device optimal for high-power satellite application.

Depending on the difficulty of achieving innovative and optimized amplification solutions, the inevitable result is elaboration of nonlinear models adapted of the new model equivalent circuit element in Fig. 1 of the transistors, capable of the precisely and efficiently predicting evolution of the HEMT model [8] as a function of the input power based on genetic algorithm estimates.

The recent studies provide only qualitative and contradicting explanations of the trapping phenomena [10-12]. That places the circuit designers in a very tough situation: on the one hand, the trapping effects problems cannot be solved rapidly by the development of HEMT technology; on the other hand, until now, none of the trap models has been available in commercial tools. This is the basis to find an accurate and efficient way to characterize these trapping effects, which can be used by the circuit designers.

In this section, first the state of the physical explanation for trapping effects will be selected. Next, the model that can take the trapping effects into account will be presented.

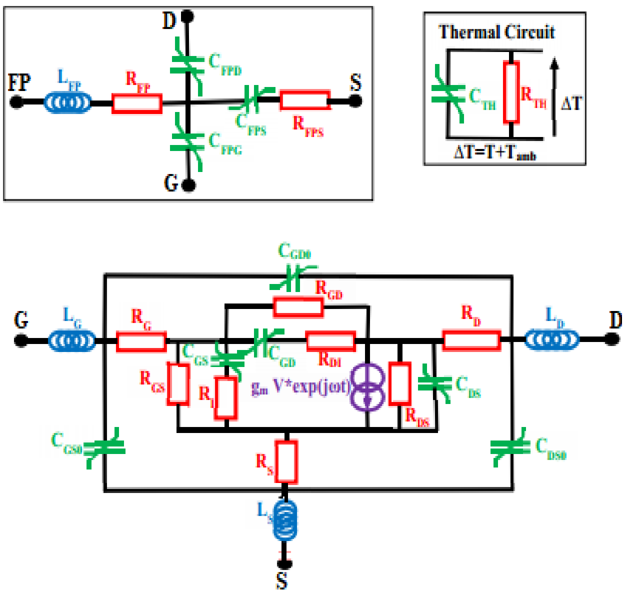

Fig. 1. Equivalent nonlinear small signal model of FP-HEMT integrating thermal effects [3, 9].

This work describes the method that enables to find the customized extensive extract to the thermal model under conditions of low trapping, to correctly predict the reactive currents in the device. The extraction model and parameters of the simulated device include some kind of effects inherent to trapping mechanism, either the self-heating with small scale space in this device, or the hot electrons spilled over from the potential trapped by the defects in barrier and buffer layers [4].

The first step is extraction of the parasitic inductances parameters of all the proposed circuits. Hence, the Z-parameters can be expressed as follows:

$$Z_1 = j\omega L_G\,,\ Z_2 = R_G\,,\ Z_3 = j\frac{\left(\dfrac{1}{j\omega C_{GD}} + R_{DI}\right)\times R_{GD}}{\left(\dfrac{1}{j\omega C_{GD}} + R_{DI}\right) + R_{GD}}\,,$$

$$Z_4 = R_D\,,\ Z_5 = j\omega L_D\,,\ Z_6 = \frac{R_{GS}\times\left(\dfrac{1}{j\omega C_{GS}} + R_I\right)}{R_{GS} + \left(\dfrac{1}{j\omega C_{GS}} + R_I\right)}\,,$$

$$Z_7 = \frac{\dfrac{1}{j\omega C_{DS}}\times R_{DS}}{\dfrac{1}{j\omega C_{DS}} + R_{DS}}\,,\ Z_8 = R_S\,,\ Z_9 = j\omega L_S\,,$$

$$Z_{10} = \frac{1}{j\omega C_{GS0}}\,,\ Z_{11} = \frac{1}{j\omega C_{GD0}}\,,\ Z_{12} = \frac{1}{j\omega C_{DS0}}\,. \qquad (1)$$

In the second step, we extract the remainder of the circuit, which includes the field plate and back bulk, with their effects:

$$Z_{13} = R_{FP} + j\omega L_{FP}\,,\ Z_{14} = \frac{1}{j\omega C_{FPS}} + R_{FPS}\,,$$

$$Z_{15} = \frac{1}{j\omega C_{FPG}}\,,\ Z_{16} = \frac{1}{j\omega C_{FPD}}\,,\ Z_{17} = \frac{1}{j\omega C_{GDA}}\,. \qquad (2)$$

The fundamental output power including the current dispersion and thermal characteristics of the analytical models for HEMTs has been simulated in different works [13-15], but the new approach here is to simulate a device with addition of effect elements of the field plate electrode and the back bulk. When we thought about creating an integrated structure for our system, we worked on choosing all the features that fit our requirements, so that the device can adapt in a thermal environment.

In the gate structure without field plate, the gate resistance increases [16], drop in the gate-source and gate-drain capacitances (fringing capacitance, C_{GF}) [17] decreases, and the device gives the lowest output power density and power added efficiency.

Therefore, we added field plate structure with the *T*-gate to benefit from its performance:

- Recess process [18] and passivation layer over the gate increase C_{GF}, which results in smaller f_T and $f_{\max}$.
- Increasing the intrinsic electron velocity (v_e) [18], which limits the decrease in f_T, but the passivation layer between the gate and field plate increases the fringing capacitance (C_{GF}) considerably and results in lowest $f_{\max}$ [16].
- Increasing the output power and efficiency [19].

The cross-section of our FP-HEMT structure is presented in Fig. 2. A layout of different layers is the same classical structure of HEMT [20], with addition of the Fillip Chip mode and field plate electrode.

The self-heating effect is one of the main reasons for restricting performance in III-N materials based devices. It not only affects the output power, but also affects the reliability of the device. Many methods for reducing the self-heating effect were reported, such as changing the substrate material [21, 22]. In this paper, 4H-SiC is used as the substrate and back bulk layer, which greatly reduces the self-heating effect. This simulation is made by TCAD-Silvaco software analysis of $In_{0.185}Al_{0.815}N$/AlN/GaN, the self-heating mode scan is carried out to study the impact of temperature on the device.

The 2D map of the lattice temperature is presented in Fig. 2b, the temperature in the device with self-heating reaches the maximum temperature close to 559 °C in the gate, which shows the effectiveness of the design in restricting heat and allowing to reduce it on the source electrode. The high stability of the lattice between InAlN and GaN strained structures may allow demonstrating high temperature operation in a temperature regime not yet accessible to FETs [23]. These properties should then also be favorable to obtain high speed performance due to the low parasitic one.

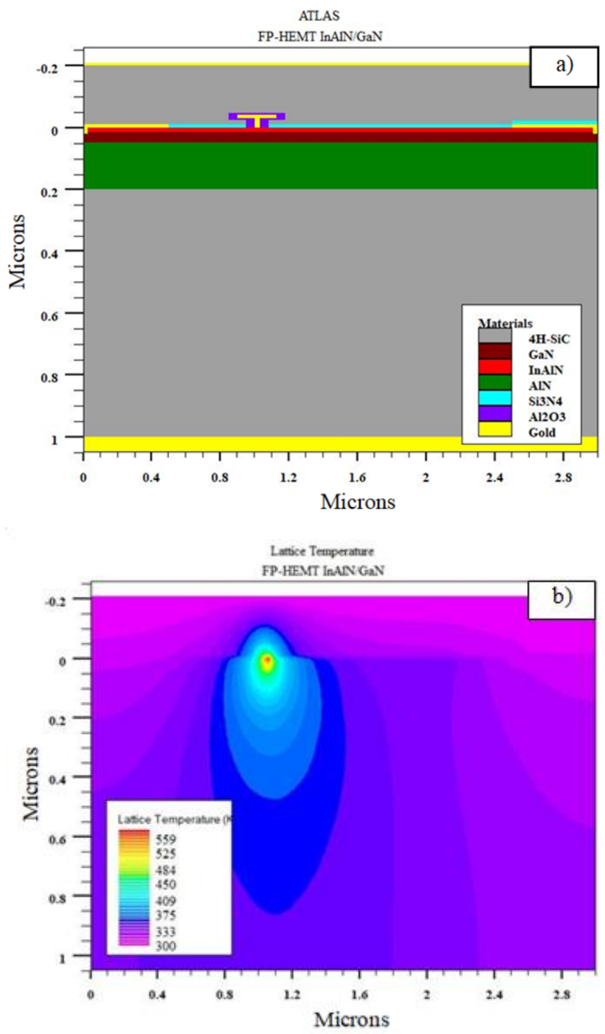

Fig. 1. a) 2D schematic cross-section of FP-HEMT. b) Scan 2D of lattice temperature at V_{DS} = 5.0 V and V_{GS} = 0.

3. Results and discussion

We will highlight the possibility of extending our principle of modeling for simulation at high power levels up to the point of compression of gain. In this case, retro-simulation of large Ku frequency band power amplifiers will ultimately allow us to conclude on the precision brought by our model under space operational conditions of optimization of the power efficacy and their performance.

The methodology we have adopted to exploit the modeling results is based on the ability of the Silvaco-Tcad simulation benchmark of the pulsed *I*/*V*, AC, RF and *S* characteristics to reproduce finely the differential characteristics of transistors with a local negligible error.

3.1. DC characteristics

Modeling the performance of the small signal model based on hydrodynamic physical models for simulation is seen in Fig. 3, where the *I*–*V* characteristic is demonstrated. The good agreement in simulation indicates the ability of the proposed model to describe the DC performance of the device.

The Schottky contact between the gate in gold and the thin InAlN barrier layer increases the electron density in the channel by steering gate voltage performance [24]. The carrier concentration is very low in the channel, when the gate voltage is less than or equal to the threshold voltage, and consequently the drain current is almost zero.

To be able to suppress the leakage towards the substrate of the current which circulates from the source to the drain and to exhaust the 2DEG channel of confined electrons, a negative voltage bias is applied to the gate from 0 to –8 V. The pinch-off voltage is extract from the transfer characteristic, as shown in Fig. 3a; its value is about –2.5 V. The increasingly negative pinch-off voltage means higher amount of power consumed during the on/off state transition [25]. Due to high electron mobility at low temperatures, the current increases very quickly with the increment of V_{DS} in the linear region. As the temperature goes up, the electron mobility decreases.

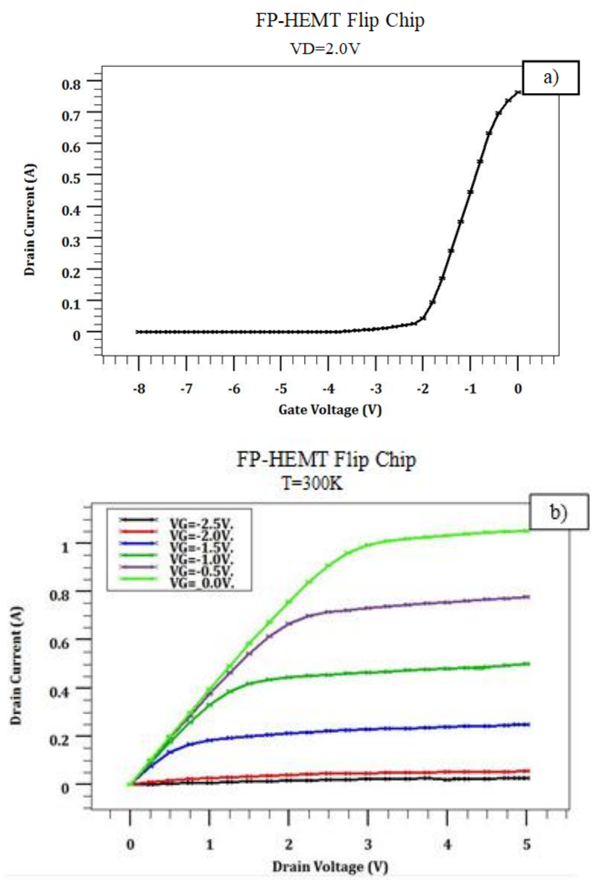

Fig. 2. Hysteresis curves characteristics for (a) linear coordinate system transfer input, and (b) output curves for FP-HEMTs with V_{GS} increasing from –2.5 V to 0.

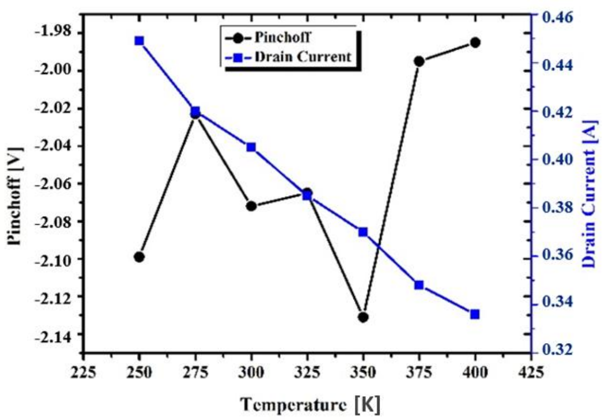

Fig. 4. Pinch-off voltage and *I–V* characteristic *versus* the temperature for FP-HEMT.

We confirm that the *I–V* characteristics keep the same features relatively well behaving as compared to other HEMTs [26, 27]. The maximum source drain current is about 1050 mA/mm, and an on-state resistance (R_{ON}) of 2.82 Ω·mm at V_{GS} = 0.0 (Fig. 3b).

Fig. 4 shows the output characteristic and the pinch-off voltage of the HEMT *versus* the temperature at V_{DS} = 2.0 V. We see that the saturation region starts at higher I_{DS} values at lower temperatures. The results show that the proposed device exhibits stable operation at high current levels (~450 mA/mm at 300 K, and 330 mA/mm at 400 K). At low temperatures, the HEMT presents a substantial enhancement in performance, over room temperature.

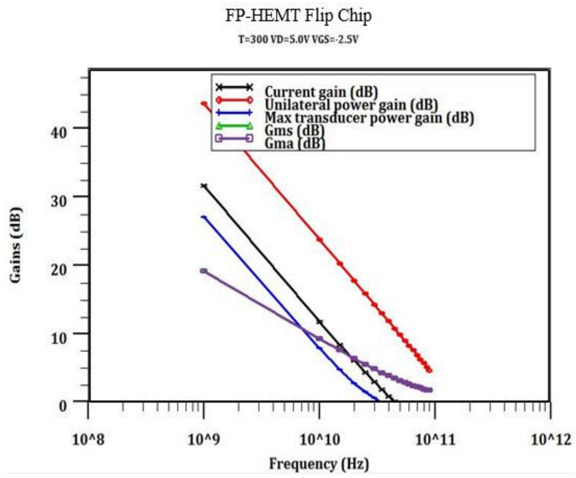

Fig. 5. AC characteristics for FP-HEMT.

The pinch-off voltage largely depends on the gate capacitance; so a decrease in gate capacitance with temperature between 250 and 400 K, which implies a relevant efficiency of using an Al_2O_3 dielectric layer in the HEMT gate. A small change in the threshold voltage due to the temperature variation causes a significant change in the output current.

Basically, we can see that the device hence performs a stable characteristic for high current operation with temperature.

3.2. AC characteristics

These good static characteristics are coupled with a cutoff frequency f_T higher than 45 GHz. The frequency f_{GMA} is approximately 105 GHz, the frequency of the max transducer power gain is very important factor for operation in RF regime f_{GMT} = 34 GHz, and the maximum frequency $f_{\max}$ is higher than 110 GHz. That allows very efficient operation at low drain polarization. All the gain characteristics for the device (Fig. 5) are for V_{GS} = 0.0 and V_{DS} = 5.0 V at room temperature.

This device shows higher performance than that of a conventional one. The reasons for these results are mainly due to the higher transconductance and the higher output resistance resulting from a graded polarization in the InAlN barrier (30 nm) and the back-bulk layers.

In Fig. 6, we report the variation of cut-off frequency and maximum oscillation frequency as a function of the temperature. From 250 up to 400 K, the cut-off frequency decreases and the maximum oscillation frequency increases. The slopes of the linear part fitted of the InAlN on SiC device in $f_{\max}$ are 283/250 GHz/K to 295/400 GHz/K, and for f_T 27/250 GHz/K to 49/400 GHz/K. Owing to the very small DC-to-RF dispersion, variation of f_T and $f_{\max}$ with temperature is

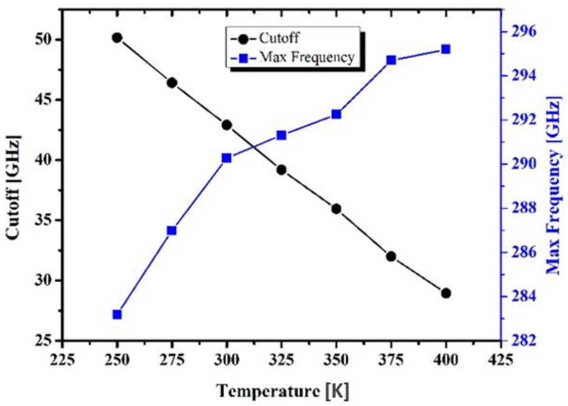

Fig. 6. AC characteristics *versus* temperature for FP-HEMT.

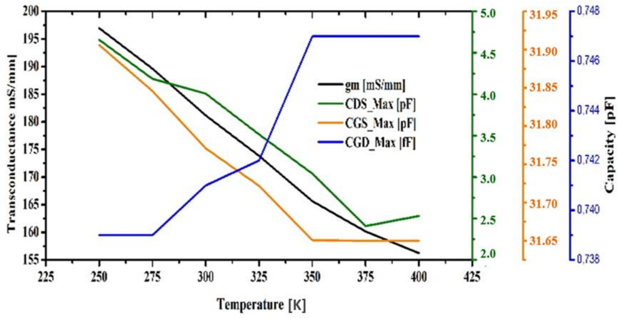

Fig. 7. *C*–*T* and *gm*–*T* characteristics for FP-HEMT.

achieved even with a relatively low DC. In addition, a high $f_{\max}/f_T$ ratio can be obtained, due to the low gate resistance and high C_{GS}/C_{GD} ratio. In the channel, the reflection in effective electron velocity is monotonic with increasing the temperature, which leads to a decrease in the cut-off frequency [28].

The element parameters of back bulk and low coupling effect between access lines as Al_2O_3 and the gate minimize the impact on the device [29]. This result confirms that the back bulk has practically no influence on the HEMT frequency performance.

In high frequency and high-temperature operation conditions, the investigation of capacitance is extremely valuable and requires a thoughtful consideration.

The intrinsic gate capacitance and the trans-conductance extracted from the small-signal model are presented in Fig. 7. The GaN material based HEMTs suffer from trapping effects that hamper the achievable output power; the trapping effect phenomena observed in GaN HEMTs are very complex and are not completely understood yet.

In low frequencies, R_I and C_{GS} have small values for low noise devices. The capacitances C_{GS} and C_{DG} present a nonlinear dependence on both voltages V_{GS} and V_{DS}. The transconductance falls sharply with increasing the gate length. This type of device exhibits remarkably enhanced performance at low temperatures because of the improvement in the electron transport properties [32].

3.3. S-parameters

We selected the parasitic elements of both the extrinsic and intrinsic parameters of the small-signal simulated device model; **we determine by minimizing the error in *S*-parameters**. Optimization of simulation is given for a device in the Ku frequency band. That proposed method is suitable to determine exactly parasitic parameters of new model with excellent fit of *S*-parameters. Since this condition is fulfilled, the results of pulsed [*S*] simulations enable to extract precisely all the device elements. The intrinsic capacitances are first extracted from the bias-dependent *S*-parameter simulations using an optimizer-based extraction [5, 6].

The circuit proposed in Fig. 1 has been used to reproduce the dispersive behavior observed when simulating the intrinsic *S*-parameters plotted in Fig. 8.

The extrinsic parameters have not embedded from all the simulations used for the purpose of device modeling. Therefore, the extrinsic parameters are extracted and de-embedded according to [31]. This simulation has been carried out in the frequency pulse range at the Ku frequency band, where the heat has a direct effect on the operation mode of the device which enables a detailed analysis of all the factors. Although the temperature is changed inside the device in accord with the self-heating data, the parameters S_{21} have not a few been observed by the bearing changes.

In contrast, the results obtained with the proposed circuit model successfully reproduce the device performance in all the frequency range (including the low-frequency deviations in S_{11} and S_{22}). In this case, all elements of the circuit are kept with the same values, and the additional R_{TH} and C_{TH} have been optimized to properly reproduce the device response at low frequencies. In particular, they fit the dispersion of the apparent R_{DS} and *gm* parameters, and have an estimation of the characteristic frequency of the traps, which in this case corresponds to the Ku frequency band.

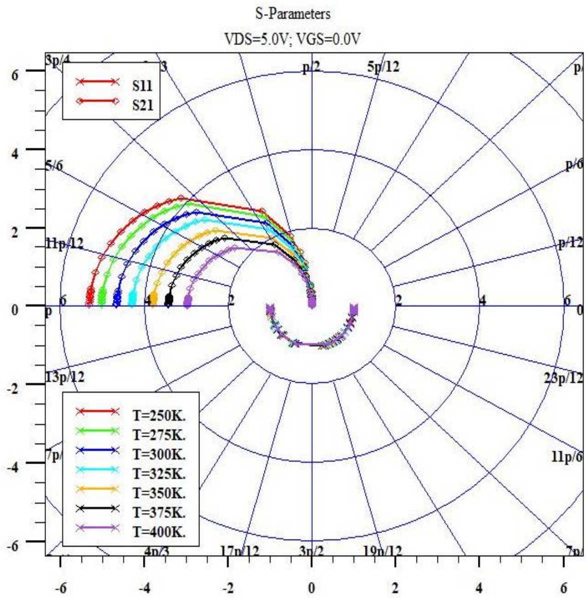

Fig. 8. *S*-parameter with the temperature effect (T = 250 K up to 400 K).

4. Conclusion

This work presents an approach where simulation with Tcad-Silvaco is used to reduce the search space of solutions by using a new circuit proposed with this programming to address the FP-HEMT characterization of the thermal effect and power device application in space.

The above points summarize the proposed approach when working out the analytical program used for the linear model, and the solution is the optimal position to each transistor problem.

The search for a final model of the best equivalent circuit element has been created, and we validated the parameter extraction process for the correct model. The proposed model demonstrates its viability in high power and high temperature space applications.

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Нова модель малого теплового сигналу для FP-HEMT, що використовується для супутникового зв'язку

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Анотація. У цій статті досліджено транзистор із високою рухливістю електронів, керований електричним полем (FP-HEMT), з пасивацією оксидом алюмінію, узгодженням ґраток InAlN/GaN та затвором довжиною 30 нм. Змодельовано оцінку його характеристик в залежності від режиму теплового впливу. Також проаналізовано і змодельовано цей пристрій запропонованою еквівалентною схемою, яка враховує міжелектродний розподілений зовнішній паразитний та додатковий внутрішній зворотний зв'язок. Потім проведено дослідження, як цей пристрій можна використовувати в теплових умовах, типових для супутникового зв'язку. Програмне забезпечення симулятора Tcad-Silvaco використано для прогнозування результатів оцінки характеристик, заданих за допомогою генетичного алгоритму, для поліпшення часу обчислень і точності моделі. Отримані результати підтверджують припустимість використання цієї нової моделі пристрою з тонким бар'єром InAlN, Filip Chip і польовою пластиною в одній структурі в режимі сигналу підсилювача високої потужності на геостаціонарній тепловій орбіті.

Ключові слова: транзистор із високою рухливістю електронів, керований електричним полем (FP-HEMT), тепловий ефект, телекомунікаційний супутник, посилення потужності.