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Physics of microelectronic devices

The advancement of silicon-on-insulator (SOI) devices and their basic properties

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Abstract. Silicon-on-insulator (SOI) is most promising present-day silicon technology. The use of SOI provides significant benefits over traditional bulk silicon technology in fabrication of many integrated circuits (ICs), and in particular, complementary metal-oxide-semiconductor (CMOS) ICs. It also allows extending the miniaturization of CMOS devices into the nanometer region. In this review paper, we briefly describe evolution of SOI technology and its main areas of application. The basic technological methods for fabrication of SOI wafers are presented. The principal advantages of SOI devices over bulk silicon devices are described. The types of SOI metal-oxide-semiconductor field-effect transistors (MOSFETs) and their basic electrical properties are considered.

Keywords: silicon-on-insulator (SOI), metal-oxide-semiconductor field-effect transistor (MOSFET), multiple-gate transistor, ultra-thin-body SOI transistor, fully-depleted SOI transistor, interface coupling.

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1. Introduction

As known, almost every modern electronic device, such as a laptop, mobile phone, smartphone, *etc*., is built using the silicon Integrated Circuits (ICs), and in particular, Complementary Metal-Oxide-Semiconductor (CMOS) ICs, the main building block of which is the silicon Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). For a long time, CMOS ICs were fabricated solely on the bulk Si substrates. However, it was later found that the use of Silicon-On-Insulator (SOI) instead of Si wafers in manufacturing CMOS ICs provides a number of important advantages, namely: increased reliability and radiation hardness, extension of the operation temperature range, reduction of parasitic capacitances, improvement of the device performance and operation speed, *etc*. [1-8]. In the recent two decades, the rapid development of SOI CMOS device technology has been primarily driven by its ability to overcome the fundamental obstacles that arise in bulk Si CMOS technology in MOSFET downsizing to nanometer dimensions [9-18], and also to reduce device operation voltage and power consumption, which makes it very attractive for modern computing and communication systems [19-26].

In the 1970–80s, application of SOI technology was mainly limited by manufacturing CMOS ICs capable to operate under extreme conditions (at ionizing radiation and high temperatures) intended for use in aerospace, nuclear and military industries [1-8]. The main obstacle to the widespread use of SOI was the lack of high-quality SOI wafers and their high cost. To the end of the 20th century, SOI applications began to grow rapidly and entered the mainstream ultra-large-scale ICs. It is explained by several reasons. One is that SOI wafers have become commercially available and less expensive. The other is related to the fact that by this time bulk Si CMOS technology reached its limit in terms of MOSFET miniaturization, and the use of SOI technology made it possible to continue reducing the MOSFET's length down to $L_g \leq 10$ nm gate length [9-11, 13-18]. One more important reason for the sharp increase of SOI market is growing use of SOI in consumer portable and mobile electronic devices, such as laptops, mobile phones, smartphones, *etc*., which require high-speed, low-voltage and low-power operation [23-27].

Currently, SOI is the leading technology for manufacturing ICs and key electronic components for many mainstream electronic applications, including computing devices, wireless communication systems, Internet services, *etc*. SOI is used for manufacturing ultra-low-power digital, analog, radio-frequency (RF), and mixed-mode integrated circuits. One of the largest modern SOI applications is fabrication of high-performance processors [23-25]. A large share of SOI market falls on RF Front-End Modules (FEMs).

According to Global Forecast, this segment of SOI market will continue to grow over the next five years due to growing demands to RF FEMs in the new generation mobile communication systems, such as 5G as well as in consumer electronic devices, such as smartphones, laptops and tablets. Nowadays, almost all smartphones, including 2G, 3G, and 4G, use SOI-based RF chips, which enable faster and more reliable data transmission [27]. SOI structures are also extensively used in Micro-Electro-Mechanical Systems (MEMS) and Nano-Electro-Mechanical Systems (NEMS), chemical and biological integrated sensors, optical waveguides and photonic circuits, *etc*. [3, 23, 28-31]. In addition, SOI structures are used to realize new types of devices, namely: three-dimensional (3D) ICs [2, 3, 32, 33], new memory cells based on floating-body effects [34-35], novel quantum-effect devices, for instance, single-electron SOI transistor, quantum-wire SOI transistor, *etc*. [36-38].

In this review, we will consider the key advantages of SOI CMOS devices over bulk Si counterparts. Basic technologies for producing the SOI wafers will be outlined. Various types of SOI MOSFETs will be described. The specific electrical properties of fully and partially depleted SOI MOSFETs will be considered.

2. Principal advantages of SOI CMOS devices over bulk Si devices

Among the modern silicon ICs, the dominant role belongs to complementary metal-oxide-semiconductor ICs, in which each logic element consists of a pair of complementary *p*- and *n*-channel MOSFETs. In traditional bulk Si-based CMOS technology, isolation of integrated circuit elements from one another is provided by reverse-biased *p*-*n* junctions. However, this approach has many drawbacks. Isolation by using *p*-*n* junctions increases parasitic capacitance and leakage currents, limits the packing density of elements and leads to parasitic coupling between circuit components, which enhance with increasing the packing density and reducing the size of elements. This problem can be solved by using the SOI substrates instead of bulk Si wafers [1-4].

A schematic cross-sectional view of a typical SOI wafer is shown in Fig. 1. The thickness of Si film depends on the type of future application; it can be t_{Si} = 10…20 nm (for nanoscale CMOS applications), or it can be tens of micrometers thick (for power devices or micro-electro-mechanical systems).

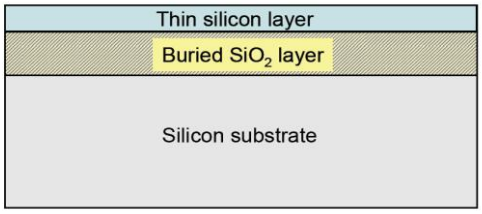

Fig. 1. Schematic cross-sectional view of a SOI wafer.

Unlike traditional bulk Si technology, in SOI technology, the IC elements are formed not in bulk silicon substrate but in separate islands of thin silicon film lying on a dielectric and being dielectrically isolated from each other (Fig. 2). Full dielectric isolation of the elements in SOI CMOS ICs provides significant reduction in parasitic capacitances and prevents a number of parasitic effects inherent to bulk Si CMOS devices. Described below are the most important advantages of SOI CMOS devices over bulk Si counterparts.

2.1. Enhanced reliability and radiation hardness of SOI CMOS devices to transient radiation effects

Elimination of latch-up effect. One of the most serious problems of bulk Si CMOS ICs is the *latch-up* or *parasitic thyristor effect*. This phenomenon consists in creation of a low-impedance path resulting from unintentional triggering of the *n*-*p*-*n*-*p* parasitic thyristor structure inherent to bulk Si CMOS devices. The occurrence and theory of latch-up effect, as well as the methods to reduce its influence, are widely covered in numerous articles and textbooks on physics and technology of ICs [1, 2, 39-42]. Since in CMOS devices, *p*- and *n*-channel MOSFETs must be produced on the same substrate, in bulk Si technology, it requires formation in the substrate the regions with the type of conductivity opposite to that in the substrate and called as "*wells*" (Fig. 2a). As a result, in bulk Si CMOS devices there is always a four-layer *n*-*p*-*n*-*p* parasitic thyristor structure formed by n^+-type source/drain regions of *n*-MOSFET, *p*-substrate, *n*-well, and p^+-type source/drain regions of *p*-MOSFET (Fig. 2a). This *n*-*p*-*n*-*p* parasitic thyristor structure can be presented by two bipolar *n*-*p*-*n* and *p*-*n*-*p* transistors, the collector of each of which is connected to the base of the other. If one of two bipolar transistors gets forward biased due to excess current flowing through the well or substrate, the other also turns on. Because of the positive feedback between the *n*-*p*-*n* and *p*-*n*-*p* transistors, latch-up can occur; therewith the low-impedance state becomes self-maintaining until the power supply voltage is interrupted. It results in a temporary loss of the device functioning or irreversible device damage. The latch-up can be induced by different factors including ionizing radiation, heavy-ion strikes, spikes in the supply voltage, powerful microwave interference, temperature increase, *etc*. The latch-up is the most common failure mechanism for bulk Si CMOS ICs, and with increasing the packing density and decreasing IC element sizes, which decreases transistor spacing, this problem is aggravated [39-42].

In SOI CMOS devices, there are no wells; *p*- and *n*-channel MOSFETs are isolated from each other and from the silicon substrate by the dielectric. Thus, in SOI CMOS devices there is no parasitic thyristor structure (Fig. 2b), and therefore they are inherently immune to latch-up effect. Because of this, SOI CMOS ICs are much less sensitive to voltage spikes, temperature fluctuations, or pulse irradiation than bulk Si CMOS circuits [1-3].

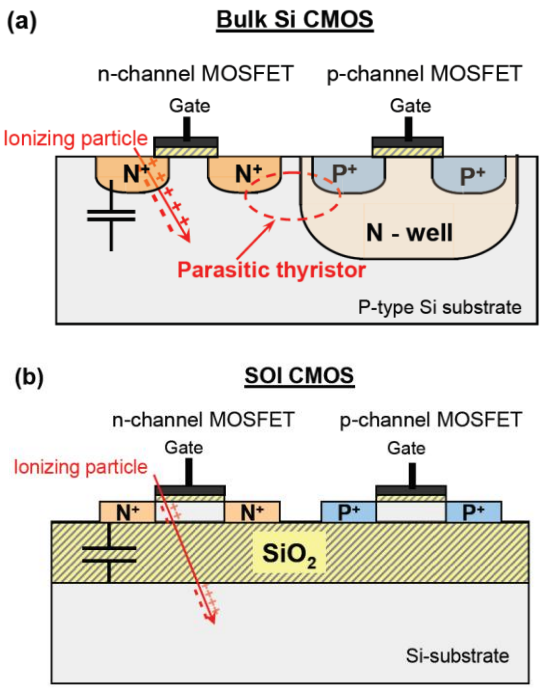

Fig. 2. Schematic representation of CMOS transistors based on bulk Si (a) and silicon-on-insulator (SOI) (b).

Reduced ionization currents. High radiation hardness to transient ionizing radiation exposure and ionizing particles (electrons, protons, alpha particles) is an essential advantage of SOI CMOS devices as compared to their bulk silicon counterparts [2, 5, 8, 43, 44]. Transient radiation effects (radiation-induced breakdown, latch-up effect, *etc*.) are the device responses to significant ionization currents. In SOI devices, ionization currents (or photocurrents) are considerably lower than in their counterparts on bulk Si due to the small volume of the active region, much smaller regions of *p*-*n* junctions, as well as due to the presence of buried SiO_2 layer, which prevents the flow of charges generated in the substrate into the active area of the device (see Fig. 2b) [2, 8].

However, SOI CMOS devices, similar to their bulk counterparts, are sensitive to the total (cumulative) dose effects associated with accumulation of radiation-induced charge in the gate dielectric layer and generation of interface states at the Si/dielectric interface. These effects can be minimized by reducing the thickness of the gate dielectric and using the radiation-resistant dielectrics. In addition, in SOI CMOS devices, there is a specific problem related to radiation-induced positive charge accumulation in the buried SiO_2 layer, which can result in the parasitic conduction channel at the Si film/buried SiO_2 interface in the *n*-channel MOSFETs [44-47]. This problem can be solved using deep ion implantation to increase the doping concentration in the lower part of the Si film and thereby increasing the threshold voltage of the back parasitic transistor [45, 46], as well as by application of the negative substrate bias under irradiation [45-47].

An alternative method to solve this problem is to replace the buried SiO_2 layer with a three-layer SiO_2–Si_3N_4–SiO_2 dielectric featuring essentially weakened radiation-induced charge accumulation [48, 49].

2.2. Reduced parasitic capacitances and higher operation speed

In CMOS devices, the most important parasitic capacitance is the capacitance between the source/drain regions and the substrate, which in the case of bulk devices is the capacitance of *p*-*n* junctions (Fig. 2a). Miniaturization of MOSFETs, which in conventional bulk Si technology requires an increase of doping concentration in the substrate or around *p*-*n* junctions, leads to an increase of parasitic capacitances of *p*-*n* junctions in bulk CMOS devices. Reduction of supply voltage, which is relevant for modern electronic devices, in bulk CMOS circuits also increases the parasitic drain capacitance. In thin-film SOI CMOS devices, where the regions of *p*-*n* junctions extend up to the buried SiO_2 layer, the parasitic capacitance of junctions represents the capacitance of a MOS structure formed by a highly doped region of the *p*-*n* junction, buried dielectric, and substrate (Fig. 2b). The maximum value of this capacitance is equal to the capacitance of the thick buried dielectric layer, being proportional to its dielectric constant. The dielectric constant of SiO_2, which is most often used as a buried dielectric, is approximately three times less than the dielectric constant of Si, and therefore, the capacitance of the drain and source junctions in SOI CMOS devices is much lower than in their bulk Si counterparts [1, 2, 50, 51]. Besides, in SOI devices, the parasitic capacitance can be further reduced using a high-resistivity Si substrate [52, 53].

Parasitic capacitances in SOI CMOS devices are much less sensitive to downscaling the elements, since the thickness of the buried oxide and the doping concentration in the substrate may remain unchanged. In addition, the parasitic capacitances of the *p*-*n* junctions in thin-film SOI devices are considerably less sensitive to lowering the supply voltage. The presence of the thick buried oxide between a thin silicon layer and silicon substrate in SOI devices reduces not only the parasitic capacitances of the drain/source *p*-*n* junctions, but also other parasitic ones, such as the capacitance between the conductive tracks and substrate, the gate and substrate, *etc*. Significant reduction in the total parasitic capacitance in SOI devices provides a strong increase of their operation speed as compared to that in bulk counterparts [2, 50, 51].

2.3. Reduced supply voltage and power consumption

The SOI technology enables effective reduction of the IC supply voltage and power consumption as compared to bulk Si CMOS technology [2, 19-22]. Thin-film fully depleted SOI MOSFETs feature a sharper subthreshold slope of the transfer characteristic than bulk MOSFETs

due to a lower value of the body-effect coefficient [2, 54-56] (see Section 5.2). It allows lower threshold voltages to be applied without increasing the off-state current, and thus allows to reduce the supply voltage of the device.

The use of SOI instead of bulk Si also provides a significant (by several times) reduction in the device power consumption. This is explained as follows. Power consumption in MOS ICs consists of static (P_{stat}) and dynamic (P_{dyn}) components. The static component is determined by the power dissipation in the standby mode ($P_{stat} = I_{off} \cdot V$, where I_{off} is the drain current in the off-state of the transistor, V – supply voltage). The dynamic component caused by energy dissipation during switching of the device is approximately proportional to $P_{dyn} \sim f \cdot C \cdot V^2$, where f is the clock frequency, C – sum of the device capacitances, and V – supply voltage. Due to the significant reduction of the total parasitic capacitance and reduction of the supply voltage, the power consumption in SOI ICs is much lower than in conventional bulk Si ICs [2, 54-56]. For this reason, the SOI technology is ideally suited for manufacturing electronic components for portable electronic devices and mobile communication products, for which reduction of the power consumption is of crucial importance.

2.4. Benefits of SOI MOS devices for high-temperature operation

Many applications of electronic devices, such as automotive, aviation, nuclear, oil, gas industries and others, require operation at high temperatures. Conventional bulk silicon CMOS devices and ICs can operate only at moderate temperatures ≤150…200 °C; at higher temperatures they fail to operate because of significant increase in the MOSFETs' off-state leakage current, temperature-induced latch-up, threshold voltage shifts, and degradation of subthreshold characteristics. Thin-film SOI CMOS devices are capable to operate at temperatures up to 300…400 °C [2, 5-8, 57, 58]. It is due to several advantages of SOI devices as to high-temperature operation. The first one is the absence of temperature-induced latch-up, which is explained by the absence of the parasitic thyristor structure (Fig. 2).

Another important advantage of SOI MOSFETs is much lower off-state leakage current at high temperatures. An increase in the MOSFET off-state leakage current with temperature is one of the main factors limiting the upper operation temperature of MOS devices and circuits. In a general case, the off-state leakage current (I_{off}) in MOSFETs consists of two components: generation current (I_{gen}) associated with thermal generation of carriers in depleted regions of the reverse-biased *p-n* drain junction, and diffusion current (I_{diff}) caused by the diffusion of minority carriers from quasi-neutral regions adjacent to the depleted junction areas. Both components are proportional to *p-n* junction areas but have different temperature dependences: generation component I_{gen} varies as $\sim n_i(T)$, whereas the diffusion component I_{diff} varies as $\sim n_i^2(T)$, where n_i is the intrinsic carrier concentration in silicon, whose temperature dependence is expressed as [59]:

$$n_i(T) \sim T^{3/2} \exp\left(-E_g / 2kT\right), \quad (1)$$

where T is the temperature, E_g – silicon bandgap energy, and k – Boltzmann constant. Therefore, I_{diff} increases with temperature much stronger than I_{gen}. In bulk Si CMOS devices, I_{off} at high-temperatures is defined by the diffusion mechanism featuring the $n_i^2(T)$-dependence; therewith the major contribution comes from a very large diffusion component associated with well-to-substrate junction (see Fig. 3). In thin-film SOI devices, I_{off} in a wide temperature range is mainly defined by I_{gen} that increases with temperature as $n_i(T)$. It has been demonstrated that at high temperatures, I_{off} in SOI CMOS devices is 3-4 orders of magnitude smaller than in counterpart bulk devices. It is explained by significantly smaller *p-n* drain junction areas and the elimination of very large well-to-substrate diffusion component that is separated from the device active region by the buried oxide layer (Fig. 3), as well as by a weaker temperature dependence of I_{off} [2, 5-8, 57, 58].

An additional high-temperature advantage of thin-film SOI MOSFETs operating in a fully-depletion mode is weaker variation of the threshold voltage and subthreshold slope with temperature than in bulk MOSFETs. It is related with the absence in fully depleted SOI MOSFETs the temperature-induced variation of the depletion layer width in the subthreshold region and at the threshold [60]. Due to aforementioned high-temperature advantages, SOI devices are widely used in high-temperature electronics.

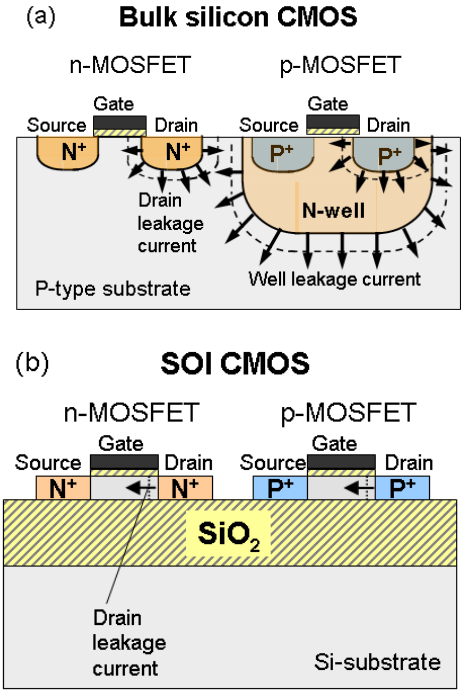

Fig. 3. Schematic illustration of the sources of the high-temperature off-state current in bulk silicon CMOS devices (a) and SOI CMOS devices (b).

2.5. Better control of short-channel effects in SOI MOSFETs

The use of SOI structures instead of bulk Si allows solving the key problem of MOSFET miniaturization in the nanometer region related to the detrimental short-channel effects. SOI-based MOSFETs of a new configuration, such as ultra-thin and multi-gate SOI MOSFETs, which feature enhanced electrostatic gate control, are less affected by the short-channel effects, and thus they can be downsized to lower dimensions. This issue is discussed in more detail in Section 4.

3. Methods for fabricating SOI wafers

Various techniques to produce SOI wafers have been developed. All of them are aimed at creating a thin monocrystalline Si layer on an insulator (usually, an amorphous SiO_2 layer), having a low defect density, high thickness uniformity, and high quality of Si/insulator interfaces. A detailed description of the various methods can be found, for example, in [2-4, 61]. The most-used techniques, which received an industrial application, are briefly described below.

Silicon-on-Sapphire (SOS). SOS is the first SOI technology that has received practical application [62, 63]. At that time, the main motivation for the development of the SOS technology was fabrication of radiation-hard CMOS ICs. SOS wafers are produced by heteroepitaxial growth of a Si film on monocrystalline sapphire (Al_2O_3) substrates. Because of the lattice mismatch and different thermal expansion constants of Si and sapphire, SOS films feature the compressive stress, a high density of crystallographic defects and the presence of an intermediate defective layer at the Si/sapphire interface. It adversely affects the electrical characteristics of SOS films, especially very thin films [64]. Several methods have been elaborated to improve quality of SOS films. Among them, the most-used is the technique called solid-phase epitaxial regrowth (SPEAR) [65-67]. In this technique, silicon implantation is used to amorphize the silicon film, excepting a thin top layer, where the initial defect density is the lowest. During the subsequent thermal annealing, solid-phase regrowth of the amorphized silicon occurs, therewith the top Si layer acts as a seed. Using this technique provides substantial reduction of the compressive stress and the defect density. The advantages of SOS are the high thermal conductivity of the sapphire substrate, which reduces self-heating effects, as well as a low parasitic capacitance and low dielectric loss tangent of the sapphire substrate. It makes SOS very attractive for microwave circuit applications [68-70]. Because of a high cost of sapphire substrates, the use of SOS technology is limited to the manufacture of devices for military and space applications, as well as high-frequency circuits.

Zone-Melting-Recrystallization (ZMR). This technique consists in recrystallization of a polysilicon film deposited onto an insulating substrate (usually, a thermally oxidized Si wafer) by scanning a narrow melt zone across the wafer. As a rule, before recrystallization, the polysilicon film is coated with a protective (encapsulating) layer of SiO_2, which prevents contamination of the melt and affects the crystallographic orientation of the recrystallized Si film [71-73].

Various energy sources are used to create the molten zone, namely: strip graphite heaters [74], powerful halogen lamps [75, 76], laser and electron beams [71-72, 77-79]. The best results have been obtained using the continuous lasers, in particular, the powerful neodymium laser YAG Nd with the wavelength of 1.06 μm. To ensure the active absorption of laser irradiation, the wafer is heated on the back to a temperature within the range 1200…1300 °C [78-80]. A schematic illustration of the ZMR method is shown in Fig. 4.

A certain level of crystallographic orientation of ZMR SOI films is provided without any special orienting factors (*i.e.*, in the spontaneous nucleation of crystals), due to the directional nature of the process. In the case of sufficiently thin films, plate-like Si crystallites are formed, being sandwiched between two SiO_2 surfaces. The (100) Si/SiO_2 interface is characterized by the lowest free energy. As a result, ZMR SOI film consists of a small number of monocrystalline silicon grains with the (100) surface orientation, elongated in the scanning direction [78-80]. The main defects in ZMR SOI films are subgrain boundaries. It has been shown that subgrain boundaries have a weak effect on the electrical characteristics of ZMR films and devices based on them. In particular, they have no effect on the threshold voltage of SOI MOSFETs and the carrier mobility; however, they cause degradation of the carrier lifetime [81, 82].

The advantages of the ZMR method are the ability to control the thicknesses of the Si film and buried oxide, and its low cost. At present, ZMR technology is used for manufacturing radiation hard SOI integrated sensors.

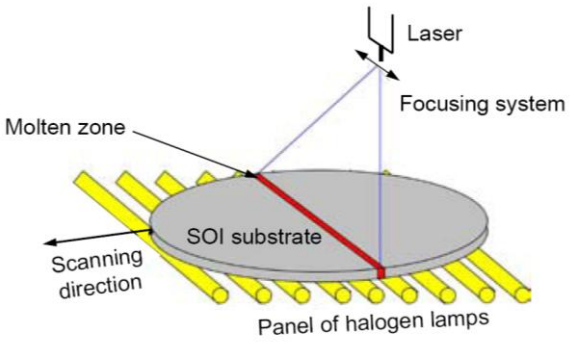

Fig. 4. Schematic illustration of the ZMR method for fabrication of SOI wafers.

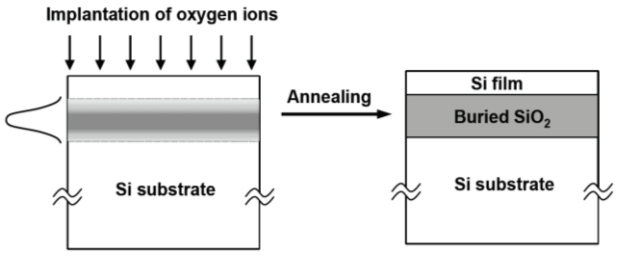

Fig. 5. Schematic representation of the SIMOX method to fabricate SOI wafers.

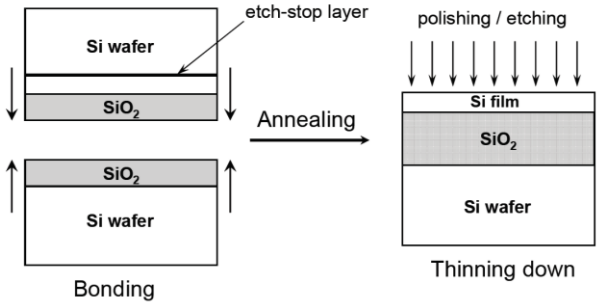

Fig. 6. Schematic illustration of the BESOI method.

Separation by IMplantation of Oxygen (SIMOX). The SIMOX method was developed by K. Izumi *et al*. at NTT (Japan) in 1978 [83]. In this method, a high-dose oxygen-ion implantation (~0.3…1.8)·10^{18} O^+/cm^2 followed by high-temperature annealing is used to create a buried SiO_2 layer. A high temperature post-implantation annealing (at $T \geq 1300$ °C for 3…6 hours) is needed to eliminate implantation defects and to provide diffusion and segregation of implanted oxygen to form a continuous stoichiometric SiO_2 layer (Fig. 5) [2-4, 61, 83-86].

In order to prevent complete amorphization of the top silicon layer during implantation, a high-dose oxygen implantation is performed at elevated temperatures (at T ~500…600 °C). In this case, due to the dynamic annealing of damages during implantation, a monocrystalline Si layer retains near the surface. The thickness of Si film in the resulting SOI structure is defined by the implantation energy, whereas the thickness of the buried SiO_2 layer is defined by the dose of oxygen implantation. In the standard SIMOX process, the implantation energy is close to 200 keV and the dose equals 1.8·10^{18} O^+/cm^2, which eventually gives a 200-nm-thick Si film and a 400-nm-thick buried oxide. In SIMOX technology, the wafer cost and residual implantation damage strongly depend on the implantation dose. For this reason, the subsequent investigations were aimed at reducing the implantation dose. It has been demonstrated that a high quality buried oxide can be obtained using the significantly lower doses within a narrow dose window (≈ 4·10^{17} O^+/cm^2) with the subsequent annealing at T = 1350 °C for 6 hours. The thickness of buried oxide in this "low-dose" SIMOX SOI structure is approximately 80 nm. The "low-dose" SIMOX technology with the high-temperature post-implantation annealing allows to obtain thin defect-free Si films on thin (80…100-nm-thick) buried oxides [87, 88]. However, quality of the buried oxide and its interfaces in SIMOX SOI wafers is worse as compared to SiO_2 layers obtained by thermal oxidation of silicon.

Wafer bonding (WB). The wafer bonding method is based on the phenomenon that two flat and clean wafers, when brought into contact, are attracted to each other by van der Waals forces and adhere or "bond" to each other, even at room temperature. Since the initial adhesion is rather weak, the bonded wafers must be annealed at high temperatures to achieve sufficient mechanical strength. The procedure of obtaining the SOI wafers by the wafer bonding method consists in the following stages: two silicon wafers, at least one of which is oxidized, are brought into close contact and annealed. Then one of two bonded wafers is thinned down by mechanical grinding, polishing and chemical etching to reach the required thickness of the Si film, whereas the other serves as a mechanical support. This technique for fabrication of SOI wafers is called BESOI (Bonded and Etch back Silicon-On-Insulator) [89-91].

In the BESOI process, the thickness of future Si film and its uniformity are usually controlled by the etch-stop layer (typically, a B- or Ge-rich layer) introduced before wafer bonding. The BESOI process is schematically illustrated in Fig. 6. The main disadvantage of the BESOI method consists in the fact that it requires two wafers to obtain one SOI wafer.

Smart-Cut® method. This method was proposed by M. Bruel from Soitec (France) and patented under the name *Smart-Cut*®. SOI wafers fabricated by *Smart-Cut*® technology received the tradename *UNIBOND*® [92-95]. Sometimes, the term "UNIBOND" is used to refer the layer splitting technique to produce SOI structures. The *Smart-Cut*® method combines ion implantation and wafer bonding approaches to transfer a thin silicon layer from one wafer to another. In this method, SOI wafers are obtained by wafer bonding followed by splitting of a thin Si layer from one of the wafers. The main steps of creating a SOI structure by using the *Smart-Cut*® method are shown in Fig. 7.

Initially, as in the wafer bonding method, two wafers of monocrystalline silicon are used, one of which is thermally oxidized. However, in distinction to the conventional wafer bonding method, prior to bonding the deep high-dose implantation of hydrogen ions (≥5·10^{16} ions/cm^2) is performed into an oxidized Si wafer (wafer 1 in Fig. 7). It results in formation of hydrogen-enriched layer at a certain depth under the oxide.

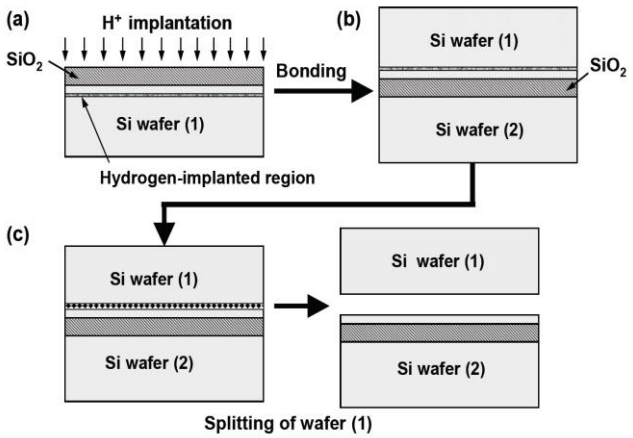

Fig. 7. Schematic representation of the main steps in the *Smart-Cut*® method of fabrication UNIBOND SOI wafers: (a) hydrogen implantation; (b) wafer bonding; (c) splitting of wafer (1) at the hydrogen-implanted layer. Wafer (1) can be reused.

The depth of this layer is defined by the implantation energy and thickness of the oxide (see Fig. 7a). After the implantation procedure, the wafers are bonded (Fig. 7b). Then a heat treatment (at $T \sim 500…600$ °C) of bonded wafers is carried out. During annealing, the hydrogen fills the implantation-induced cracks and voids, resulting in their growth and making the hydrogen-implanted region a mechanically weakened zone. Then, along this implant-damaged layer, the first wafer is separated (Fig. 7c). At the final stage of the process, chemical and mechanical polishing of the SOI film is performed to improve surface quality and obtain the required thickness of the Si film. The separated part of the first wafer can be reused (Fig. 7d) [2, 4, 92-95]. Thus, in contrast to the BESOI method, in which two Si wafers are used to produce one SOI wafer, in the *Smart-Cut*® method only one Si wafer is consumed. This is a significant benefit of the *Smart-Cut*® method. Moreover, UNIBOND SOI films obtained by using this method have excellent electrical characteristics comparable with those of bulk silicon.

Currently, *Smart-Cut*® is main industrial technology for production of SOI wafers, and Soitec (France) is the world leading industrial company producing best-quality ultra-uniform UNIBOND SOI wafers of large diameter (300 mm) [27, 96].

It is important to note that the smart-cut layer splitting technique is not limited to the manufacture of silicon-on-insulator structures for which it was originally developed. It has been also successfully used to produce thin monocrystalline films of various materials on an insulator, namely: SiC (silicon carbide-on-insulator, SiCOI) [96-98], GaAs, InP, $LiNbO_3$ [96, 98], Ge (germanium-on-insulator: GeOI) [96, 99]. It also allows creating semiconductor-on-insulator systems such as silicon-on-quartz, silicon-on-glass, silicon-on-diamond, *etc*. [2, 96].

Epitaxial Layer TRANsfer (ELTRAN). The ELTRAN method is based on the fact that porous Si is mechanically weak, and that it retains crystalline quality of the substrate on which it was formed. In the ELTRAN technique, SOI wafers are produced by combining creation of a porous Si layer, epitaxy, and wafer bonding processes [100]. The method includes the following steps. The layer of porous silicon is formed on the Si wafer by using the electrochemical etching in a solution of HF, followed by annealing in a hydrogen atmosphere. Then, an epitaxial Si layer of the desired thickness is grown on the surface of the porous silicon and thermally oxidized to form a future buried oxide. The wafer is then bonded to the second wafer. After that, the splitting of the bonded wafers along a mechanically weakened porous layer is carried out.

4. Miniaturization of MOSFETs in bulk Si technology and SOI technology

The main trend in the development of CMOS IC since their advent has been a continuous reduction of MOSFET's dimensions. Therewith, the most critical MOSFET's size is the gate length L_g, since reducing it allows not only to increase the packing density, but also to increase the operation speed. The major problem of the MOSFET downsizing is associated with detrimental *short-channel effects*, which begin to occur, when the channel length of the transistor becomes comparable to the width of the depleted regions of source/drain *p-n* junctions. In this case, the electric field distribution in the channel area under the gate becomes essentially two-dimensional, which means that the potential and carrier concentration distributions in the channel are defined not only by the transverse electric field induced by the gate, but also by the longitudinal field induced by the drain voltage. It results in an increase in the off-state leakage current, degradation of the subthreshold characteristics, and Drain-Induced Barrier Lowering (DIBL) effect [59, 101, 102]. DIBL effect consists in the lowering of the potential barrier at the source edge of the channel and forward bias of the source junction caused by the drain voltage, which leads to the threshold voltage roll-off with decreasing the channel length and increasing the drain voltage [102].

4.1. MOSFET miniaturization in conventional bulk Si CMOS technology

In conventional bulk silicon CMOS technology, the problem of "short-channel effects" for many years has been solved using the scaling approach proposed by Dennard in 1974 [103]. According to this approach, if all of the transistor dimensions and applied voltages are reduced by a scaling factor α ($\alpha > 1$), and the channel doping concentration is increased by the same factor, the shape of the electric field distribution in the scaled MOSFET remains the same as in the original device, and therefore, undesirable two-dimensional effects that cause degradation of MOSFET characteristics do not appear.

In accordance to scaling methodology, reduction of the MOSFET channel length requires decreasing the thickness of the gate SiO_2 layer and the depth of *p-n* junctions and increasing the doping concentration in the channel [59, 101, 103, 104]. The abovementioned scaling methodology has been successfully used for the miniaturization of MOSFETs for a long time. However, when the gate length approaches to the sub-100-nm region, this methodology faces a number of fundamental limitations that hamper further shrinking the transistor size. In particular, according to scaling rules, reducing the MOSFET channel length to a value of $L_g \leq 100$ nm requires thinning the gate SiO_2 layer to the thickness $t_{ox} \leq 2$ nm. The use of such thin SiO_2 layers leads to unacceptably high gate currents because of direct tunneling of electrons through the SiO_2 layer. In addition, for $L_g \leq 100$ nm, elimination of short-channel effects by using the scaling principle requires very high doping concentrations in the channel or in the vicinity of the source/drain regions ($\geq 10^{19}$ cm^{-3}), which leads to degradation of the carrier mobility and a decrease in breakdown voltage of the source/drain *p-n* junctions, as well as increases the parasitic capacitance of these *p-n* junctions, and thereby deteriorates the device speed [9, 13-15]. This has led to the development of novel approaches for further MOSFET miniaturization.

4.2. An advanced approach for MOSFET downsizing in nanometer region

An alternative advanced approach to eliminate or minimize short-channel effects in MOSFETs is *to enhance the electrostatic effect of the gate* on the channel. This approach has two major directions [9, 12-16, 18, 105, 106]:

1) **the use of new materials**, namely, gate dielectrics with high dielectric constant (high-*k* dielectrics) instead of traditional SiO_2, and metal-like gates instead of poly-Si gates [9, 12, 14, 107-111];

2) **the use of novel SOI-based MOSFET architectures** such as planar SOI MOSFETs with ultra-thin silicon film and multi-gate SOI MOSFETs [9-18, 105, 106, 112-116].

The use of high-*k* dielectrics (HfO_2, Al_2O_3, TiO_2, Ta_2O_5, ZrO_2, La_2O_3, *etc*.) allows to increase the gate capacitance without increasing the gate current. The use of metal-like gate electrodes instead of poly-Si provides an increase of the gate capacitance due to elimination of the depletion region in poly-Si. An increase in the gate capacitance means an enhancement of the electrostatic effect of the gate, which reduces the effects of drain and source.

Another strategy for elimination or minimizing short-channel effects consists in the use of new, non-classical SOI-based MOSFET structures with improved electrostatic gate control. There are two types of SOI MOSFET's structures that allow minimizing or eliminating short-channel effects, namely: planar single-gate ultra-thin-body SOI MOSFETs and multi-gate SOI MOSFETs [2, 9-18, 105, 106, 112-116].

Ultra-thin-body (UTB) SOI MOSFETs. The fully-depleted (FD) SOI MOSFET with ultra-thin silicon body is one of the most popular transistor architectures for ultimate scaling of CMOS devices [10, 12, 15, 105, 112, 113]. Though there is no strict definition, the concept of ultra-thin-body (UTB) SOI MOSFETs is usually referred to SOI devices with silicon film thickness in the channel region ≤20 nm [10, 112, 117]. Using the ultra-thin Si films in SOI MOSFETs provides effective suppression of the short-channel effects without need of high channel doping. An additional improvement of controlling the short-channel effects in UTB SOI MOSFETs is reached using a thin buried oxide and ground plate below the buried oxide, which suppresses lateral charge sharing effects through the buried oxide [118].

Multi-gate SOI MOSFETs. Multi-gate SOI MOSFETs include double-gate, triple-gate, and gate-all-around transistors [2, 11, 16-18, 106, 114-116]. It should be noted that the term "multi-gate FET" implies a field-effect transistor, in which the gate is located on different sides of the channel. In particular, the term "double-gate FET" usually refers to a field-effect transistor, where the gate is located on two opposite sides of the device channel region, while the term "triple-gate MOSFET" refers to a transistor where a single gate covers three sides of the channel region. Schematic cross-sections of different SOI MOSFET structures that enable to reduce short-channel effects are shown in Fig. 8. Below, various types of multi-gate SOI MOSFETs will be considered in more detail.

Double-gate SOI MOSFETs. The first work on double-gate transistors was published in 1984 [119]. In this work, it has been theoretically shown that short-channel effects in a planar SOI MOSFET can be significantly reduced using two gates, namely, the conventional top gate and an additional bottom gate. However, the complexity of the fabrication processes for these double-gate structures seriously limits their practical use. The first manufactured double-gate SOI MOSFET was the fully Depleted Lean-channel TrAnsistor (DELTA) [120]. The basis of this device is a tall and narrow ("fin-shaped") silicon island covered by the gate, so that the conduction channels are formed on the lateral vertical surfaces of the silicon fin. Later, this variant of double-gate transistor with vertical channels was called FinFET (Fin Field-Effect Transistor) [11, 16-18, 121]. A schematic view of FinFET is shown in Fig. 9. A significant advantage of FinFET is its relatively simple fabrication compatible with standard planar CMOS technology, along with excellent short-channel performance.

Triple-gate SOI MOSFETs. The basis of the triple-gate SOI MOSFET is a thin-film Si strip located on the insulator and covered by the gate on the three sides (Fig. 8c). Improved variants of tri-gate transistors are the so-called Π-gate and Ω-gate transistors, in which the gate electrode on the lateral surfaces deepens to some depth into the buried oxide and extends under the channel region (Fig. 8c). It can be easily obtained by a slight overetching of the buried oxide during the Si island patterning. The gate extension improves the control of the channel by the gate and thereby lowers the role of

short-channel effects [16, 18, 114-116]. As can be seen from Fig. 8c, in the case of Ω-gate configuration, the gate almost completely covers the Si island. Therefore, in terms of electrostatic gate efficiency, Ω-gate transistor structures approach gate-all-around (GAA) structures, but unlike the latter, fabrication of Ω-gate transistors is compatible with standard planar CMOS technology. Decreasing the device cross-section in the Ω-gate device allows creation of the quantum-wire SOI MOSFETs [36].

Gate-all-around (GAA) SOI MOSFETs. Gate-all-around MOSFET structure, in which the gate completely envelops the channel (Fig. 8d), theoretically provides the best electrostatic gate control of the channel region and thus is the most efficient in terms of suppression of the short-channel effects [16, 18, 116, 122]. GAA devices are usually fabricated using a column-like silicon island with a vertical channel on the lateral surface and can have a circular or square cross-section [123, 124].

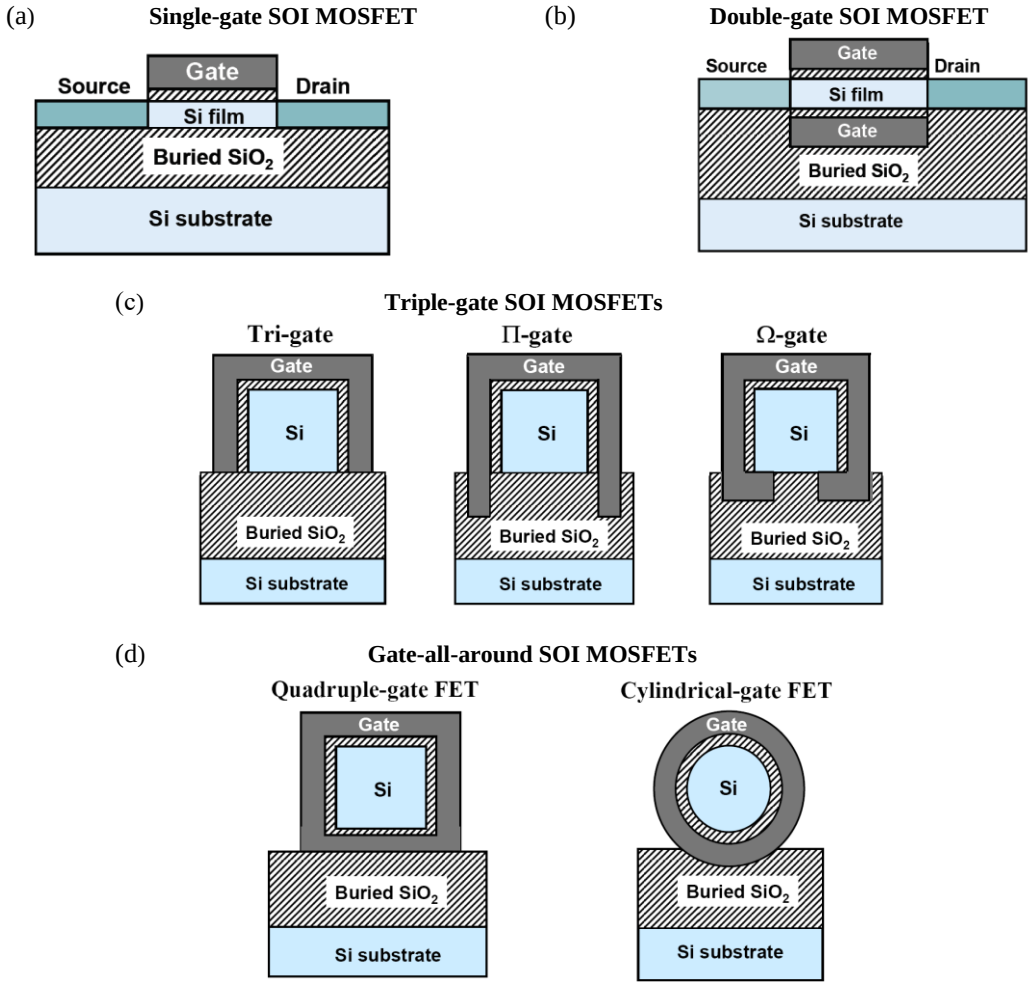

Fig. 8. Schematic views of different SOI MOSFET architectures that allow to reduce short-channel effects by improvement of the electrostatic gate control: (a) single-gate SOI FET with ultra-thin silicon film; (b) double-gate SOI FET; (c) different variants of triple-gate SOI FETs; (d) different variants of gate-all-around FETs.

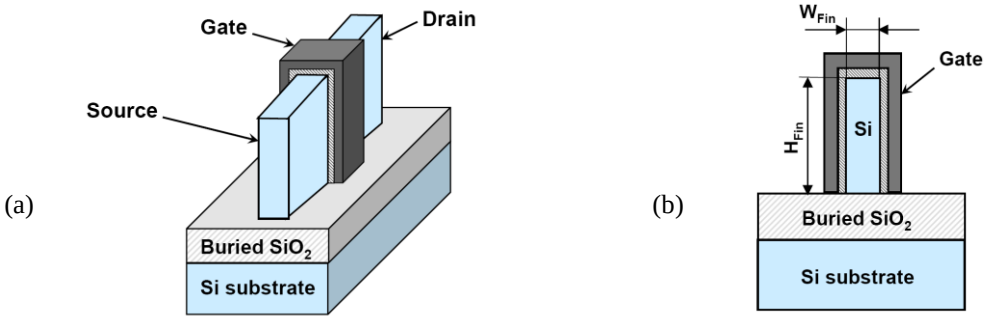

Fig. 9. General view (a) and cross-section (b) of SOI FinFET.

Junctionless SOI MOSFETs. In recent years, much attention is given to the MOSFETs without source/drain *p-n* junctions, called the "junctionless" (JL) transistors. The JL MOSFET is in fact a gated, heavily doped SOI resistor (with channel doping of $\geq 10^{19}$ cm^{-3}), which has a thin-film or multi-gate, nanowire-like structure needed to provide full depletion by the gate and thereby to turn the device off. Schematic view of the JL nanowire SOI MOSFET and its cross-section are illustrated in Figs 10a, 10b. It has been shown that, in addition to flexible, simplified fabrication process, JL MOSFETs feature excellent short-channel performance, which makes them very attractive candidates for nanoscale CMOS devices [125, 126].

Relationship between structure parameters and short-channel effects in SOI MOSFETs. To characterize the sensitivity of a particular device structure to the short-channel effects, a parameter called the "*natural length*", λ, has been introduced [16, 18, 116, 127-129]. This parameter is derived from solution of the Poisson equation and represents the length of the channel region controlled by the electric field induced by the source and drain; the smaller the value of λ, the less influence of short-channel effects. As shown by numerical simulations, for avoiding short-channel effects, the effective gate length of the MOSFET should be 5-10 times longer than λ. The parameter λ depends on the gate capacitance, gate configuration, as well as thickness and width of the Si body. The values of λ for different SOI MOSFET configurations are expressed as follows: for single-gate $\lambda_1 = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}}$ and double-gate $\lambda_2 = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{Si} t_{ox}}$ [18, 116, 127], as well as for surrounding-gate with quadruple cross-section $\lambda_4 = \sqrt{\frac{\varepsilon_{Si}}{4\varepsilon_{ox}} t_{Si} t_{ox}}$ [18, 116], where t_{Si} and t_{ox} are, respectively, the silicon and gate oxide thicknesses, ε_{Si}, ε_{ox} – permittivities of silicon and silicon dioxide. As follows from the foregoing expressions, the "natural channel length" λ, and consequently short-channel effects, can be reduced by decreasing the thicknesses of the Si film and gate oxide, and by using a high-*k* gate dielectric instead of SiO_2 (*i.e.*, decreasing the effective electrical gate dielectric thickness). Besides, the short-channel effects can be reduced by increasing a number of gates. As shown by analytical and numerical simulations, to avoid the short-channel effects, the thickness of the Si film in single-gate SOI MOSFETs with t_{ox} = 1.5 nm has to be approximately 3-4 times smaller than the gate length [16, 18, 116]. Therefore, very thin Si films have to be used for short single-gate SOI MOSFETs. However, SOI MOSFETs with $t_{Si} \leq 10$ nm show strong mobility degradation [130-133]. In addition, in such thin silicon films quantum confinement effects may cause the shift of the MOSFET threshold voltage. The use of multi-gate architecture weakens the restrictions on the Si film thickness. In the case of double-gate devices, to eliminate the short-channel effects the thickness of silicon film should be no more than 1/2 of the gate length, whereas in four-gate or surrounding-gate devices, the thickness and width (or diameter) of the silicon body should not exceed the gate length. In SOI MOSFETs with triple-gate configuration, the ratio between the gate length and the thickness and width of the Si body needed for proper control of short-channel effects is between those for double-gate and GAA devices [16, 18, 116, 129].

Though GAA MOSFET structure is the most efficient for reducing the short-channel effects, GAA devices are little used because of their manufacturing difficulties. In terms of the efficiency of the electrostatic gate control and suppressing the short-channel effects,

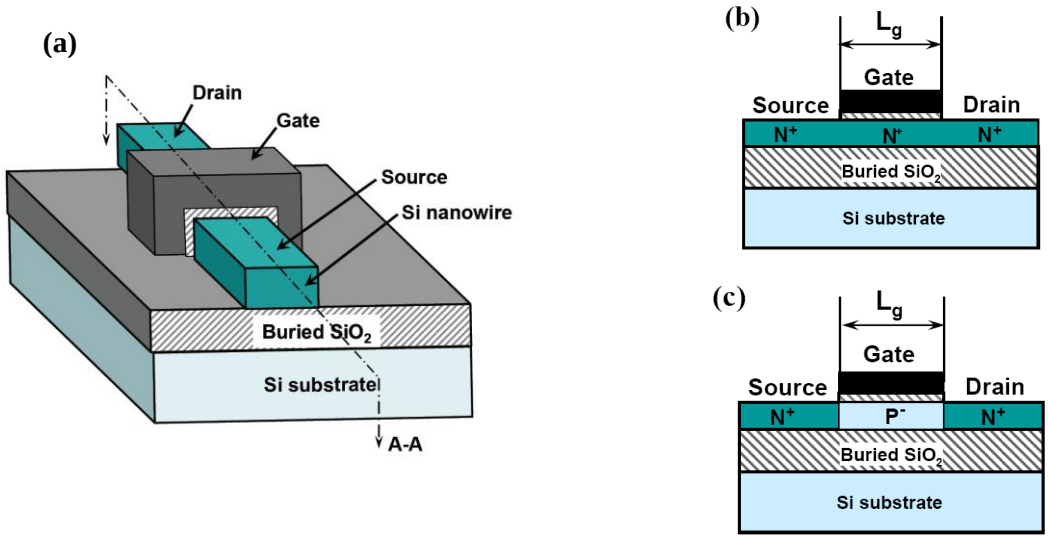

Fig. 10. (a) Schematic general view of nanowire SOI MOSFET; (b) cross-section of the junctionless *n*-channel SOI MOSFET, and (c) inversion-mode *n*-channel SOI MOSFET.

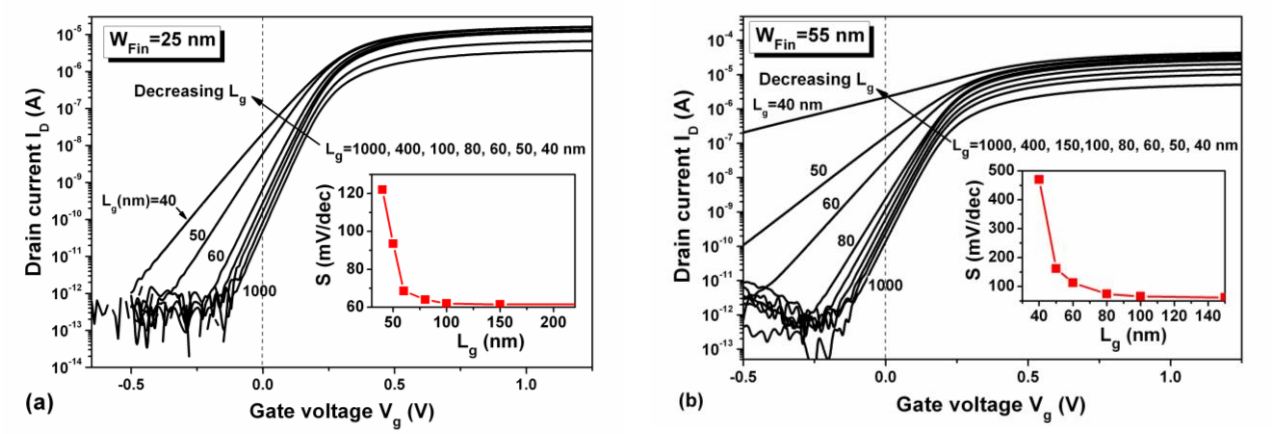

Fig. 11. Experimental drain current *vs*. gate voltage characteristics of undoped *n*-channel FinFETs with different gate lengths and two different fin widths: (a) W_{Fin} = 25 nm, and (b) W_{Fin} = 55 nm. The insets show the subthreshold slope factor as a function of the gate length. The measurements were performed at V_D = 0.02 V. The measured devices consist of 5 fins with a fin height of 60 nm and feature the SiON gate dielectric with equivalent oxide thickness EOT = 1.8 nm and a TiN gate electrode.

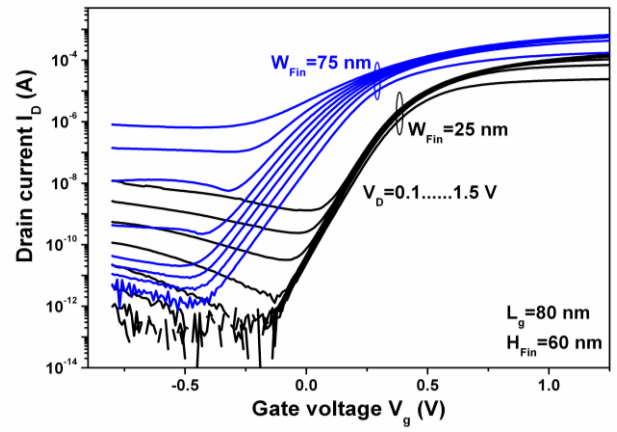

Fig. 12. Drain current *vs.* gate voltage characteristics measured in 80-nm-long FinFETs with the fin widths 25 and 75 nm at different drain voltages varying from 0.1 up to 1.5 V with 0.2 V step. It can be seen that degradation of subthreshold behavior with an increase of V_D is stronger than that in the devices with wider fins.

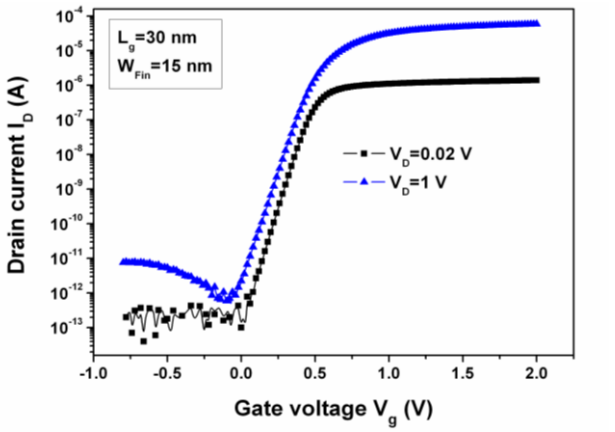

Fig. 13. $I_D(V_g)$-characteristics of the FinFET with 30-nm gate length and 15-nm fin width measured at the drain voltage of 0.02 and 1 V.

triple-gate devices lie between double-gate and surrounding-gate devices, whereas Π-gate and Ω-gate devices (see Fig. 3c) are superior to triple-gate devices and approach to surrounding-gate devices. However, in contrast to GAA devices, Π-gate and Ω-gate devices are easier to fabricate.

Since in SOI MOSFETs suppression of the short-channel effects is reached by thinning the silicon film, reducing the width of the silicon body and using the multi-gate architecture, it does not require increasing the channel doping. For this reason, modern SOI MOSFETs (excepting junctionless transistors) are usually fabricated with an undoped channel, which is advantageous from the view of the carrier mobility and elimination of parameter fluctuations associated with random dopant fluctuations. Apart from new geometry, present-day SOI FETs usually feature ultra-thin gate oxides or high-*k* gate dielectrics and metal-like "*mid-gap*" gate electrodes (*i.e.*, providing the position of Fermi level in the middle of the silicon bandgap). The most popular *mid-gap* gate materials are refractory metal nitrides, such as TiN, TaN, WN, MoN. The use of "mid-gap" gate electrodes allows providing the low and symmetric threshold voltage values in *p*- and *n*-channel SOI MIS FETs with an undoped silicon body.

Figs 11 to 13 show the impact of the fin width on the experimental short-channel characteristics of triple-gate FinFETs with undoped body and Ω-gate configuration. Fig. 11 shows behavior of the subthreshold drain current (I_D) *vs*. gate voltage (V_g) characteristics with decreasing the gate length from 1000 down to 40 nm in FinFETs with two different fin widths, namely, W_{Fin} = 25 nm (Fig. 11a) and W_{Fin} = 55 nm (Fig. 11b). The insets in Figs 11a and 11b show the corresponding gate length dependences of the inverse subthreshold slope factor *S* (*i.e.*, the value of the gate voltage needed for variation of the drain current in the subthreshold region by an order of magnitude). It can be seen that devices with a larger Si

fin width (W_{Fin} = 55 nm) show more pronounced degradation of the subthreshold characteristics with reduction of the gate length, namely, a larger degradation of the subthreshold slope and a larger rise of the off-current (*i.e.*, I_D at V_g = 0). For W_{Fin} = 25 nm, long-channel behavior with excellent S = 61…64 mV/decade is retained for the gate lengths down to L_g = 60 nm, whereas for W_{Fin} = 55 nm it is hold only to L_g = 80 nm.

Fig. 12 illustrates DIBL effects in 80-nm-long FinFETs with fin widths of 25 and 75 nm, which are revealed as degradation of the subthreshold characteristics with increasing the drain voltage. It is clearly seen that this degradation is stronger in the devices with wider fins. The value of DIBL calculated as a decrease of the threshold voltage with an increase of the drain voltage for the 80-nm long FinFET with W_{Fin} = 25 nm is only 25 mV/V, whereas for W_{Fin} = 75 nm it is 186 mV/V. For 15-nm fin width, the good control of short-channel effects is retained for the gate lengths down to 30 nm (Fig. 13). At 30-nm gate length and W_{Fin} = 15 nm, the subthreshold slope at V_D = 1 V is 69 mV/decade, which is very close to the ideal room-temperature value in the long-channel MOSFET, (*i.e.*, 60 mV/decade). On the whole, experimental data support theoretical results predicting that a good control of short-channel effects in FinFET is achieved when the fin width is ≤2/3 of the gate length [18, 116].

5. Special electrical properties of single-gate SOI MOSFETs

5.1. Partially and fully depleted SOI MOSFETs

Conventional planar SOI MOSFETs are divided into two classes, which are determined by the thickness and doping level of Si film and differ significantly in electrical properties. These are *partially depleted SOI MOSFETs* and *fully depleted SOI MOSFETs* [2, 3].

Partially depleted (PD) SOI MOSFETs. In PD SOI MOSFETs, often called as *thick-film SOI devices*, the thickness of silicon film t_{Si} is more than twice larger than the maximum depletion layer width in strong inversion, X_{d_max}, $t_{Si} > 2X_{d\_max}$, where X_{d_max} is classically expressed as [59]:

$$X_{d\_max} = \sqrt{\frac{4\varepsilon_{Si}\varphi_F}{qN_A}}, \qquad (2)$$

where $\varphi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$ is the Fermi potential, k – Boltzmann constant, T – temperature, q – electron charge, N_A – doping concentration in the channel region, and n_i – intrinsic carrier concentration. In this case, the depletion layers induced at the front and back interfaces do not extend over the whole thickness of Si film; therefore, there is always a quasi-neutral region in the Si film. If this quasi-neutral region is grounded using an additional "body contact", the electrical properties of such a SOI device will be basically the same as those of the bulk silicon one. However, if the silicon film in a PD SOI device remains electrically floating, some special unwanted phenomena called floating-body effects may occur [2, 3, 134, 135].

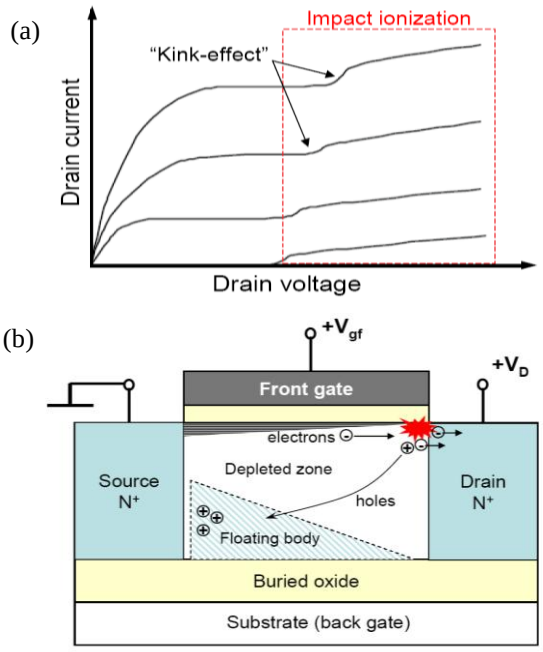

Fig. 14. Schematic illustration of the kink-effect in the *n*-channel PD SOI MOSFET: (a) drain current *vs.* drain voltage characteristics for various gate voltages in the presence of the kink-effect; (b) physical processes resulting in the kink-effect.

The typical floating-body effect in PD SOI MOSFETs is "*the kink-effect*", which is exhibited as a sharp increase of the drain current (or a kink) on the $I_D(V_D)$-characteristics at high V_D values, as shown in Fig. 14a. The physical processes responsible for the kink-effect are illustrated in Fig. 14b by the example of the *n*-channel PD SOI MOSFET. At sufficiently high drain voltages, the channel electrons can acquire a sufficient energy to cause impact ionization near the drain, which results in electron-hole generation. The generated minority carriers (electrons) flow into the drain, while the majority carriers (holes) migrate to the device body and accumulate near the source, resulting in the rise of the body potential and forward bias of the source-body *p-n* junction, which is equivalent to reduction of the threshold voltage. This brings about the stepwise increase of the drain current on the $I_D(V_D)$-curves (Fig. 14a). Since the mobility of holes is much lower than the mobility of electrons, in the *p*-channel transistors, "the kink-effect" is less than in the *n*-channel ones.

The floating body in PD SOI MOSFETs can also cause hysteresis phenomena, the effect of parasitic bipolar transistor, dynamic threshold voltage variations. The above undesirable floating-body effects can be eliminated by creating a body contact and its grounding, however, this solution is unfavorable from the manufacture point of view. An alternative approach consists in the use of thin-film, fully depleted SOI structures that are free of floating-body effects [2, 136]. On the other hand, based on the floating-body effects in SOI structures, a new type of dynamic computer memory called "zero capacitor RAM" (*Random Access Memory*) has been created [34, 35].

Fully depleted (FD) SOI MOSFET. In FD SOI MOSFETs, often called *thin-film SOI MOSFETs*, the thickness of the silicon film t_{Si} is less than the maximum depletion layer width. In this case, under threshold conditions and above threshold the Si film will be fully depleted (except for a possible thin accumulation or inversion layer at the back Si film surface, if a large positive or negative bias is applied to the substrate). Thus, in FD SOI MOSFET, the charge of the depletion layer is constant and cannot increase with increasing the gate voltage. FD SOI MOSFETs feature improved electrical characteristics as compared to partially depleted devices. In particular, they exhibit increased transconductance and carrier mobility due to the reduced effective electric field, sharper subthreshold slope caused by lower effective substrate capacitance, improved short-channel performance [2, 3, 54, 55, 137].

5.2. Subthreshold slope in partially and fully depleted SOI MOSFETs

In the subthreshold (or weak inversion) region, where the drain current rises exponentially with the gate voltage, the MOSFET operation is commonly characterized by the inverse subthreshold slope factor (or subthreshold swing) *S*. This parameter reflects the sharpness of the MOSFET transition from the off-state to the on-state and is defined as the value of the gate voltage variation required to change the drain current in the subthreshold region by an order of magnitude. Thus, by definition, *S* is given by:

$$S = \frac{dV_g}{d(\log I_D)} = \ln(10) \cdot \frac{dV_g}{d\varphi_s} \cdot \frac{d\varphi_s}{dI_D} \cdot I_D \qquad (3)$$

where φ_s is the (front) surface potential. From the classical charge-sheet model, one can obtain [59]: $I_D \cdot d\varphi_s / dI_D = kT/q$. The term $dV_g / d\varphi_s = n$, called a body factor, represents the relationship between the variation in the gate voltage and resulting variation in the surface potential. Taking this into account, *S* is usually represented as [2, 59, 54, 55]:

$$S = \frac{kT}{q}\ln(10) \cdot n = \frac{kT}{q}\ln(10) \cdot \left(1 + \frac{C_s}{C_{ox}}\right), \qquad (4)$$

where the body factor $n = (1 + C_s / C_{ox})$, C_{ox} is the (front) gate oxide capacitance, and $C_s = dQ_s / d\varphi_s$ – "effective body capacitance", *i.e.*, the capacitance between the inversion layer and the back-gate electrode or the capacitance between the inversion layer and ground in case of PD SOI device with the grounded body. The effective body capacitance C_s and a body factor *n* in bulk (or PD) SOI and FD SOI MOS devices can be found from their equivalent capacitance circuits presented, respectively, in Figs 15a and 15b.

In bulk or thick-film PD SOI MOSFETs (Fig. 15a), if the interface states are neglected, the effective body capacitance is equal to the capacitance of the depletion layer under the gate, $C_s = C_{depl}$, expressed as $C_{depl} = \varepsilon_{Si} / X_{d\_max}$, and thus the body factor *n* is:

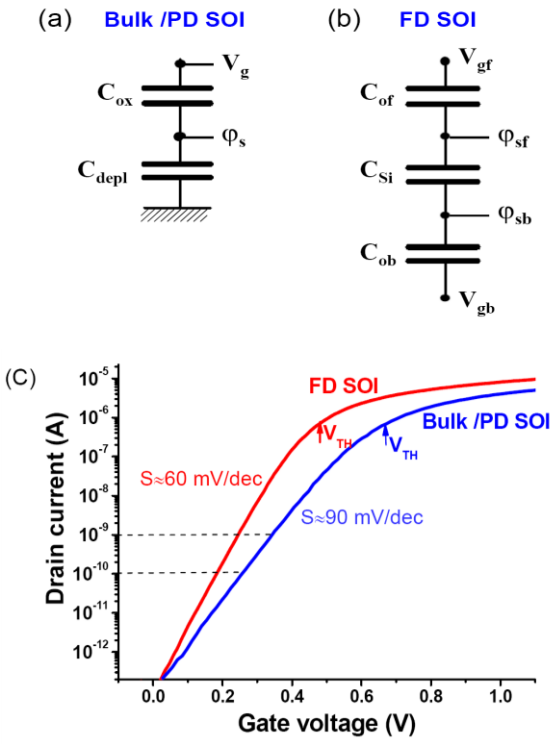

Fig. 15. Equivalent capacitance circuit of the long-channel bulk / PD SOI MOSFET (a), and FD SOI MOSFET (b). Subthreshold characteristics of FD SOI MOSFET and bulk / PD SOI MOSFET (c).

$$n = 1 + \frac{\varepsilon_{Si}}{C_{ox} \cdot X_{d\_max}}. \qquad (5)$$

The typical *n*-values in bulk or PD SOI MOSFETs lie in the range 1.4…1.6.

In FD SOI MOSFETs with depleted back Si film interface (Fig. 15b), the effective body capacitance C_s is defined by the series connection of C_{Si} and C_{ob}, where $C_{Si} = \varepsilon_{Si} / t_{Si}$ is the capacitance of the depleted silicon film, and $C_{ob} = \varepsilon_{ob} / t_{ob}$ – the capacitance of the buried oxide. This leads to the following expressions for the body factor *n* and subthreshold slope *S* in FD SOI MOSFETs (if the effect of interface traps is neglected):

$$n = 1 + \frac{1}{C_{of}}\left(\frac{C_{Si} \cdot C_{ob}}{C_{Si} + C_{ob}}\right), \qquad (6a)$$

$$S = \frac{kT}{q}\ln(10) \cdot \left[1 + \frac{1}{C_{of}}\left(\frac{C_{Si} \cdot C_{ob}}{C_{Si} + C_{ob}}\right)\right]. \qquad (6b)$$

In FD SOI MOSFETs, the buried oxide is usually much thicker than both the gate oxide and silicon film, so that $C_{ob} << C_{of}$ and $C_{ob} << C_{Si}$. It means that the second term in (6a) and the second term in brackets in (6b) are much less than unity. Therefore, when the interface trap

densities are low, in FD SOI MOSFETs with a thick buried oxide $n \approx 1$, and as a result, subthreshold slope is [2, 54, 55]:

$$S \cong \frac{kT}{q}\ln(10). \quad (7)$$

Eq. (7) corresponds to the theoretical minimum value of the MOSFET subthreshold swing, being at room temperature approximately 60 mV per decade of current. Thus, FD SOI MOSFETs feature smaller subthreshold swing than that of bulk Si or PD SOI devices, as illustrated in Fig. 15c. As a result, a lower threshold voltage can be used in FD SOI devices without increasing the off-state leakage current, which is advantageous in terms of ultra-low-power applications.

5.3. Effect of interface coupling and threshold voltage in fully depleted SOI MOSFETs

The effect of coupling between the front and back SOI interfaces is a fundamental property of any fully depleted SOI MOSFET [2, 3, 138]. This effect originates from the fact that the potential and charge distributions in FD SOI MOSFETs are actually controlled by the two gates: the front (*i.e.*, conventional) gate and the silicon substrate, acting as a second (*i.e.*, back) gate. The coupling of these surface potentials depends on the structure capacitances (see Fig. 15b) as well as on the interface properties such as interface trap density and fixed oxide charges. The interface coupling significantly affects the electrical characteristics of thin-film semiconductor-on-insulator structures and devices. In particular, due to the interface coupling, the threshold voltage in FD SOI MOSFETs depends on the substrate (or back gate) bias and on quality of the back Si film interface, and thus it may differ essentially from the threshold voltage of a bulk Si MOSFET with the same channel doping and the same gate dielectric. The effect of the interface coupling is widely used to extract the parameters of SOI structures and devices, in particular, the thickness of the silicon film and buried oxide, as well as the density of interface states [3, 82, 139]. It is also used in SOI CMOS ICs with dynamically adjustable threshold voltage ("*back-gate-controlled schemes*") [140, 141]. Moreover, the effect of the interface coupling has a wide use in SOI-based chemical and biological sensors [142-144].

5.3.1. Lim and Fossum model

Interface coupling in FD SOI MOSFETs is traditionally characterized by the so-called "coupling characteristics" that represent the dependence of threshold voltage at one gate on the opposite gate bias, which are usually described by the classical Lim–Fossum model proposed more than thirty years ago [138]. In the Lim–Fossum model, as in the classical theory of MOSFETs [59], the criterion of the threshold voltage is considered to be achieving the surface potential equal to $2\varphi_F$, where $\varphi_F = (kT/q)\ln(N_A)/n_i$ is the Fermi potential of the silicon film. According to the Lim–Fossum model, in a FD SOI MOSFET (Fig. 16a) the threshold voltage at one gate varies linearly with the opposite gate bias as long as the opposite silicon film interface is depleted and saturates with onset of strong accumulation or inversion at the opposite interface. It is assumed to occur when the surface potentials at the accumulated and inverted interfaces are 0 and $2\varphi_F$, respectively. By the Lim–Fossum model, the top (front) gate threshold voltage V_{THf} in the long-channel FD SOI MOSFET (when neglecting interface states) can be expressed as follows:

$$V_{THf} \cong V_{THf}^{acc.b} - \frac{C_{Si}\cdot C_{ob}}{C_{of}\left(C_{Si}+C_{ob}\right)}\left(V_{gb}-V_{gb}^{acc.b}\right) = \\ = V_{THf}^{inv.b} - \frac{C_{Si}\cdot C_{ob}}{C_{of}\left(C_{Si}+C_{ob}\right)}\left(V_{gb}-V_{gb}^{inv.b}\right), \quad (8)$$

where $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the capacitance of fully depleted Si film; C_{of} and C_{ob} are, respectively, the capacitances of the front-gate oxide and buried oxide (see Fig. 16a); $V_{gb}^{acc.b}$, $V_{gb}^{inv.b}$ – back gate voltages corresponding to the onset of strong accumulation and inversion at the back Si film surface; $V_{THf}^{acc.b}$ is the front-gate threshold voltage at the accumulated back Si film interface, and $V_{THf}^{inv.b}$ – front-gate threshold voltage at the inverted back Si film interface, which are expressed as [138]:

$$V_{THf}^{acc.b} = V_{FB}^{f} + \left(1+\frac{C_{Si}}{C_{of}}\right)\cdot 2\varphi_F - \frac{Q_{depl}}{2C_{of}}, \quad (9)$$

$$V_{THf}^{inv.b} = V_{FB}^{f} + 2\varphi_F - \frac{Q_{depl}}{2C_{of}}, \quad (10)$$

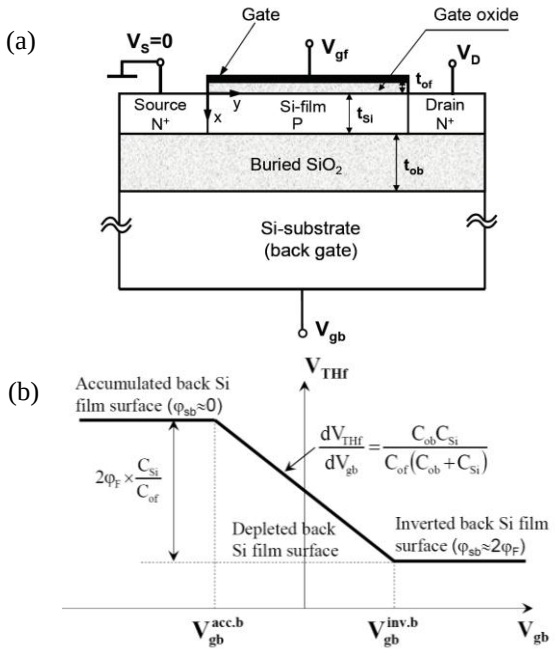

Fig. 16. (a) Cross-section of SOI MOSFET. (b) Schematic representation of the front-channel threshold voltage V_{THf} as a function of the back-gate voltage V_{gb} in a long *n*-channel FD SOI MOSFET predicted by the Lim–Fossum model [138].

where V_{FB}^{f} is the flat band voltage at the front interface; $Q_{depl} = -qN_A t_{Si}$ – density of the depletion charge per unit gate area. As it follows from (8), at the depleted back Si film interface, the front-gate threshold voltage V_{THf} varies linearly with the back-gate voltage V_{gb}, and the slope of the linear region is given by:

$$\frac{dV_{THf}}{dV_{gb}} = -\frac{C_{Si}C_{ob}}{C_{of}\left(C_{Si}+C_{ob}\right)} . \quad (11)$$

The total variation of V_{THf} with V_{gb}, *i.e.*, with the back interface potential varying from accumulation to inversion, is predicted to be $2\varphi_F\left(C_{Si}/C_{of}\right)$. Schematic representation of the V_{THf} *vs.* V_{gb} dependence (*i.e.*, the front-gate coupling curve) expected from the Lim–Fossum model is presented in Fig. 16b.

5.3.2. Special features of interface coupling in ultra-thin SOI MOSFETs

The Lim–Fossum model was successfully used for a long time and is frequently employed up to the present, because it provides simple, closed-form expressions for the device threshold voltage in terms of the opposite gate bias and structural parameters. However, over time, it was found that in the case of advanced SOI MOS transistors featuring lightly-doped ultra-thin silicon films (with $t_{Si} \le 20$ nm) and ultra-thin gate dielectrics (with the equivalent oxide thickness ≤2 nm), there are significant deviations from this model [117, 145, 146]. One of these deviations is the absence of saturation on the experimental coupling curves, which has been explained by the fact that for very thin silicon films, the electric field in the silicon film corresponding to the gate decoupling becomes too high to be achievable before the gate dielectrics damage [117]. Other distinctions are higher threshold voltage values, a steeper slope and significant extending of the linear region of the coupling curve compared to the Lim–Fossum model. Using the numerical simulations in classical and quantum-mechanical (QM) modes, it has been shown that the above differences originate from electrostatic and field-induced quantization effects [145, 146]. Comparison of the front-gate coupling curves in ultra-thin SOI MOSFET (with $t_{Si} = 11$ nm) obtained by numerical simulations performed in classical and QM modes with the Lim–Fossum model is presented in Fig. 17. A simple analytical model for the interface coupling in low doped ultra-thin-body SOI MOSFETs, which takes into account the above-mentioned effects and perfectly fits simulation and experimental results, is proposed in [146].

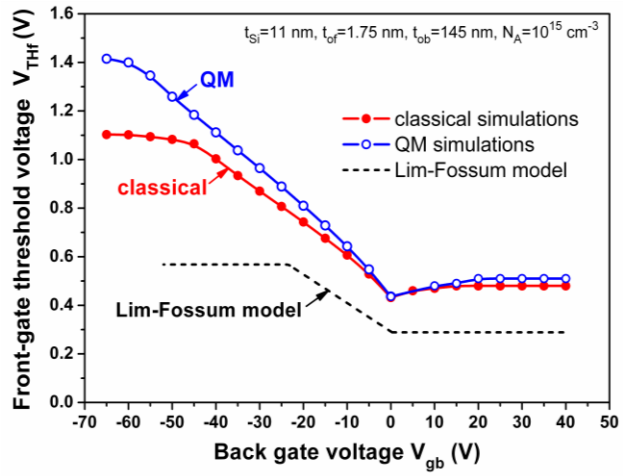

Fig. 17. Comparison between front-gate coupling characteristics of the *n*-channel ultra-thin SOI MOSFET (with $t_{Si} = 11$ nm, $t_{of} = 1.75$ nm, $t_{ob} = 145$ nm, and $N_A = 10^{15}$ cm^{-3}) obtained by 1-D numerical simulations in classical and quantum-mechanical (QM) modes, using the on-line available Schrödinger–Poisson solver (SCHRED) [147], and predicted by the classical Lim–Fossum model [138]. In simulations, the threshold voltage was defined as the gate voltage at which the second derivative of the inversion charge in respect to the gate voltage shows a maximum.

5.3.3. Drain current and transconductance characteristics in FD SOI MOSFETs

Apart from impact on the threshold voltage in FD SOI MOSFETs, the interface coupling results in modification of the behavior of traditional characteristics of MOSFETs [2, 3, 148]. It is illustrated in Fig. 18 that shows typical drain current I_D and transconductance g_m characteristics measured as a function of the front-gate voltage V_{gf} in the *n*-channel FD SOI MOSFET at different back-gate (*i.e.*, substrate) voltages V_{gb}. It can be seen from Fig. 18 that the shape of the characteristics of FD SOI MOSFETs is highly dependent on the back-gate bias. A lateral shift of the characteristics along the V_{gf}-axis with the back-gate bias is caused by variation of the threshold voltage. A slight change in the transconductance maximum with V_{gb} is related to variation in the effective carrier mobility caused by changes in the transverse electric field. Saturation of the characteristics in Fig. 18 with negative back-gate bias is related with accumulation at the back Si film interface, which leads to stabilization of the back-surface potential and, as a result, to saturation of the threshold voltage and transverse electric field. Appearance on the $I_D(V_{gf})$-characteristics of a linear region with a lower slope (Fig. 18a) and a plateau on $g_m(V_{gf})$-characteristics (Fig. 18b) in the range of negative V_{gf} at high positive V_{gb} is related to the formation of the inversion channel at the back Si film surface induced by variation of the front-gate voltage. These features are used to discriminate the front and back conduction channels and separately characterize the two silicon film interfaces in FD SOI MOSFETs [3, 148].

It should be noted that in the case of ultra-thin SOI devices, the two slopes on the $I_D(V_{gf})$-curves and a plateau on the $g_m(V_{gf})$-curves associated with the back conduction channel are not clearly pronounced, due to the comparable front-gate oxide and silicon film capacitances, which hampers separation of the front- and back-channel conduction regions. In ultra-thin SOI MOSFETs, channel separation can be realized using an analysis of the gate-to-channel capacitance C_{gc} *vs.* the front-gate voltage characteristics for various back-gate biases and their derivatives [145, 149].

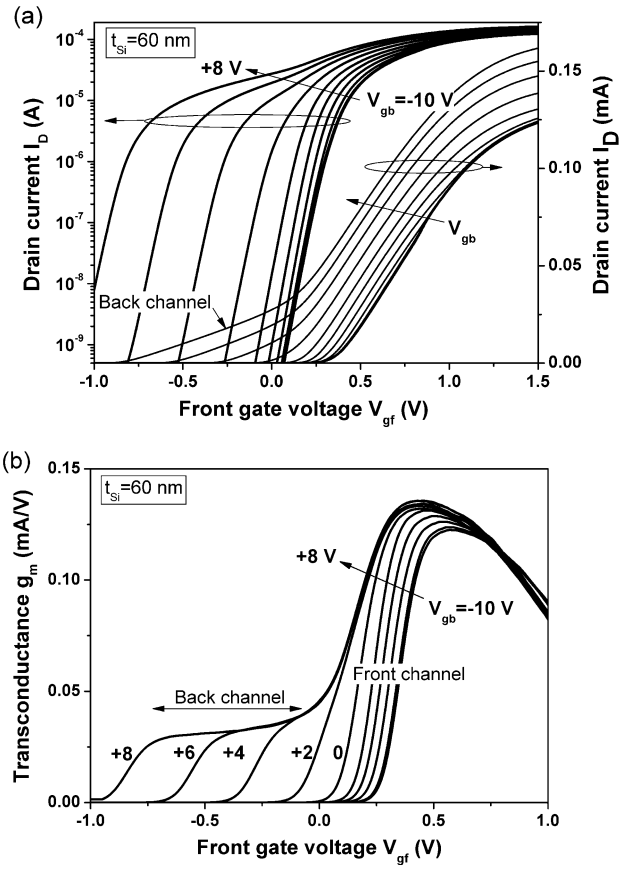

Fig. 18. Experimental drain current I_D in linear and semilogarithmic scales (a) and transconductance g_m (b) as a function of the front-gate voltage V_{gf} in the long-channel *n*-type FD SOI MOSFET at different back-gate (substrate) voltages V_{gb} (the thicknesses of the silicon film and the buried oxide are t_{Si} = 60 nm and t_{ob} = 145 nm, respectively; the equivalent gate oxide thickness t_{EOT} = 1.6 nm; N_A = 10^{15} cm^{-3}; W/L=3/1 μm; V_D = 20 mV).

5.4. Quantum-mechanical effects in ultra-thin and narrow SOI MOSFETs

In the classical theory of bulk Si MOS devices, it is assumed that the electrons (or holes) at the Si/SiO_2 interface can be treated as a three-dimensional electron gas (3-DEG) of free particles governed by the Boltzmann statistics. On the other hand, it is well known that at strong inversion when the inversion carriers are confined in the narrow triangular potential well induced by the electric field at the Si–SiO_2 interface, their motion in the direction along the normal to the interface is quantized, and thus they should be treated as a two-dimensional electron gas (2-DEG) rather than 3-DEG [150, 151]. QM effects are important when the electron wavelength in the confinement direction is comparable to or less than the spatial confinement length, which in the case of bulk Si MOSFETs is defined by the surface electric field. In particular, in bulk Si MOSFETs, carrier energy quantization affects transport properties at high gate biases and results in an increase in the threshold voltage in the devices with high substrate doping and ultra-thin gate dielectrics [152, 153].

QM effects play an important role in the electrical properties of nanoscale SOI devices, even at room temperature. In contrast to bulk Si MOSFETs, quantization effects in SOI MOS devices are affected by the presence of two potential barriers at the top and bottom Si/SiO_2 interfaces, and are defined by both structural and electric-field-induced carrier confinement. For this reason, quantum effects in SOI MOSFETs are highly dependent on the thickness of the Si film and can result in novel phenomenon such as volume inversion [154-156]. QM effects are especially important in the SOI devices with Si film thicknesses less than 10 nm. Below, we will consider some of the most important QM effects in SOI MOS devices.

5.4.1. Impact of quantum-mechanical effects on the threshold voltage in ultra-thin SOI MOSFETs

One of the most well-known QM effects in SOI MOSFETs with very thin Si films is an increase in the threshold voltage, which depends on the Si film thickness. According to classical theory, the threshold voltage of FD SOI MOSFET decreases with decreasing the silicon film thickness due to reduction of the depletion charge density Q_{depl}, being proportional to the product of film thickness t_{Si} and doping level [138]. However, this is true as long as the silicon film is thick enough. As the thickness of silicon film decreases below a critical value (about 10 nm), the conduction band splits into subbands and the minimum energy of electrons in the conduction band increases. It leads to an increase in the threshold voltage that increases with decreasing Si film thickness. This effect was first predicted by Y. Omura *et al.* in 1993 [157] and later confirmed by simulation and experimental results obtained by several groups [156, 158]. Fig. 19 schematically illustrates variation of the threshold voltage of a SOI MOSFET with the Si film thickness, obtained in [157] by simulations in the classical approximation and taking into account QM effects under the assumption of room temperature and zero back-gate bias. As seen from Fig. 19,

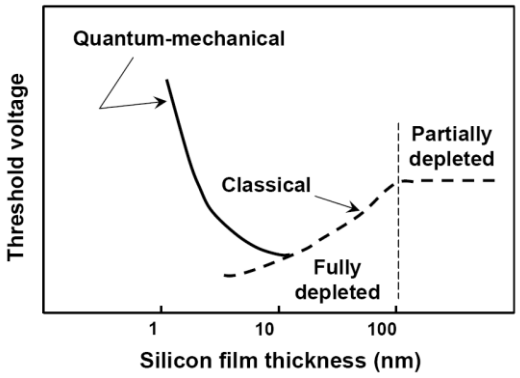

Fig. 19. Qualitative representation of the threshold voltage variation with the Si film thickness in a SOI MOSFET obtained in [157] with classical and quantum-mechanical models (on the assumption T = 300 K, N_A = 10^{17} cm^{-3}, and V_{gb} = 0).

in the classical approximation, the threshold voltage monotonously decreases with decreasing t_{Si} under conditions of full depletion of the silicon film. At the same time, the threshold voltage calculated taking into account QM effects shows an increase with decreasing t_{Si} at values less than a certain critical value (~10 nm). It is explained by the increase in the ground state energy E_0 and the decrease in the effective density of electronic states in the conduction band due to 2-D quantization caused by geometrical confinement.

As previously noted in Section 5.3, QM effects in SOI MOSFETs affect the variation of the threshold voltage with the opposite gate bias due to transformation of the potential well at threshold conditions, resulting in an increased slope of the coupling characteristics. Since this QM effect is mainly caused by the electrical confinement, it is important even for relatively thick SOI MOSFETs (with $t_{Si} > 10$ nm), whose threshold voltage is usually considered to be unaffected by quantization effects [145, 146].

Quantization-induced increase of the threshold voltage related to the geometrical confinement is also observed in thin and narrow nanowire-like triple-gate and GAA SOI MOSFETs [18, 159-161]. In thin and narrow nanowire-like SOI MOSFETs (namely, with nanowire thickness and width <10 nm), the carrier movement is confined not only in the vertical but also in the horizontal direction. As a consequence, an increase of the ground state energy in the conduction band ΔE_0 and the resulting increase of the threshold voltage in these devices are higher than that in planar thin-film SOI transistors with the same Si film thickness.

5.4.2. Volume inversion effect

One of the most important features of thin-film fully depleted SOI MOSFETs resulting from interface coupling and QM effects is the so-called *volume inversion* effect. The concept of *volume inversion* in double-gate SOI MOSFETs was first introduced in 1987 [154]. Volume inversion takes place when the distance between the potential wells induced at each Si/SiO_2 interface is so small that two inversion layers are not pressed to one of the interfaces but are spread throughout the whole Si film thickness. This feature is illustrated in Fig. 20 showing the electron concentration distributions across the Si film thickness in symmetric double-gate SOI MOS structures with different film thicknesses and the same doping concentration ($N_A = 10^{16}$ cm^{-3}) at the same total carrier density $N_{tot} = 2 \cdot 10^{11}$ cm^{-2}, obtained using an analytical quantum-mechanical model proposed in [162].

If the Si film thickness in a double-gate SOI MOS structure is larger than the total width of depleted regions induced by two gates, there is no interaction between the two inversion layers. In this case, the drain current in the double-gate SOI MOSFFET can be represented simply as a parallel combination of the front and back channels. However, when t_{Si} decreases, interaction between top and bottom potential wells arises, which raises the potential and the minority carrier concentration in the middle of silicon film. As a result, at some thickness (for the parameters in Fig. 20, at $t_{Si} \le 30$ nm), the inversion carrier concentration across the entire Si film exceeds the doping concentration. In this case, the inversion layer is not confined at the interfaces, but extends over the whole Si film thickness, which means *volume inversion regime*. Further reduction of the Si film thickness leads to a decrease in the depth of the surface potential well, resulting in a more uniform carrier concentration distribution. When the Si film is very thin (t_{Si} =10 nm in Fig. 20), the inversion carrier distribution can exhibit one maximum located in the middle of the Si film.

For the same t_{Si}, the effect of volume inversion is more pronounced at low carrier densities. It is illustrated in Fig. 21, which shows evolution of electron concentration distributions with the growth of the total electron density N_{tot} in DG SOI MOS structures featuring different silicon film thicknesses. In the case of thick SOI films (Fig. 21a), in which interaction between these two interfaces is weak, the inversion channels are formed near the interfaces, and their evolution is similar to that in a bulk MOS structure.

Another behavior is observed in the case of thin SOI films, in which interaction between these two interfaces is strong (Figs 21b, 21c). In this case, at low N_{tot}, a larger part of the carrier density is located in the central part of the Si film. With an increase of N_{tot} above a certain value depending on t_{Si}, the carrier distribution splits by two maxima. At sufficiently high N_{tot}, the contribution of surface channels to the conduction of DG SOI MOSFETs becomes dominant, and the role of volume inversion becomes insignificant; the thinner the Si film, the higher N_{tot} at which the transition from volume to surface conduction operation mode occurs.

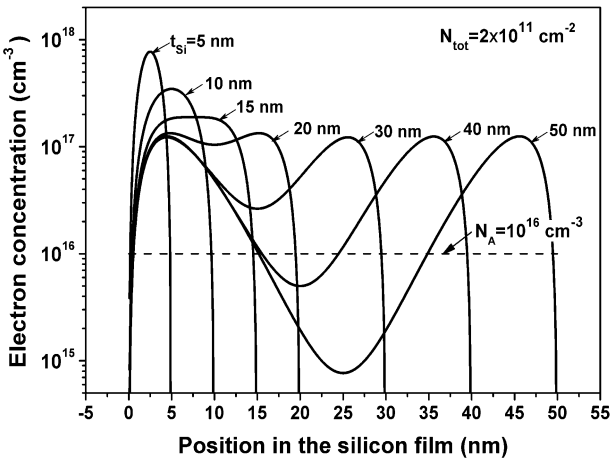

Fig. 20. Electron concentration distributions across the Si film thickness in symmetrical double-gate SOI MOS structures with different Si film thicknesses and doping concentration $N_A = 10^{16}$ cm^{-3} at the total carrier density $2 \cdot 10^{11}$ cm^{-2}, obtained using the analytical quantum-mechanical model proposed in [162].

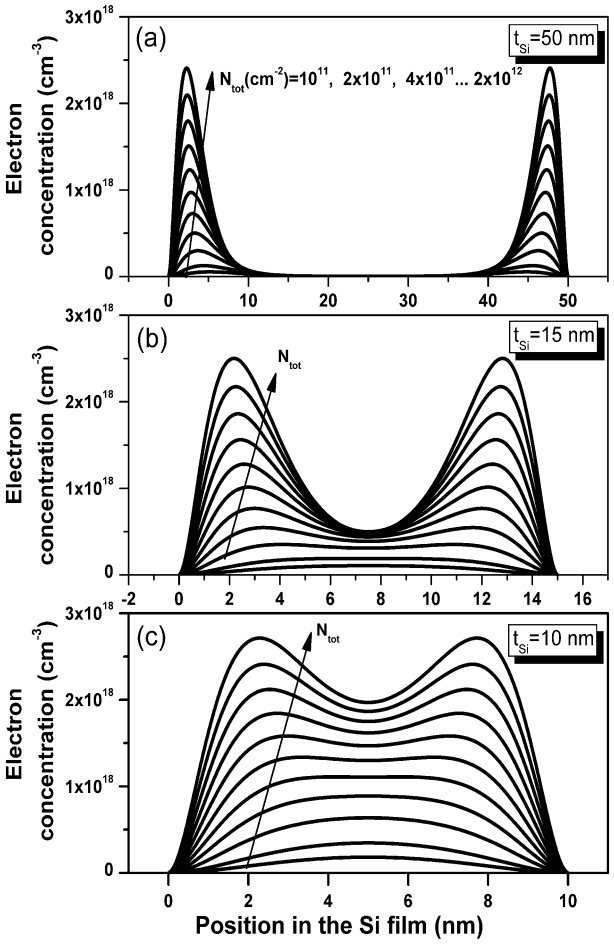

Fig. 21. Variation of the electron concentration distributions in the Si film with an increase of the total electron density N_{tot} from 10^{11} cm^{-2} to $2{\cdot}10^{12}$ cm^{-2} in DG SOI MOS structures featuring different silicon film thicknesses: (a) t_{Si} = 50 nm, (b) t_{Si} = 15 nm, (c) t_{Si} = 10 nm ($N_A = 10^{16}$ cm^{-3}).

The volume inversion effect can be observed in FinFETs, triple-gate and gate-all-around SOI MOSFETs. It has been demonstrated that volume inversion provides an improvement of the MOSFET characteristics, namely: an increase of the carrier mobility, enhancement of the MOSFET transconductance and on-state current, reduction of low-frequency noise as well as reduction of hot-carrier effects [3, 133, 154, 163].

5.5. Carrier mobility in SOI MOSFETs

The carrier mobility is a key parameter that characterizes the transport properties of charge carriers in MOSFETs. As known, the presence of the Si/SiO_2 interface significantly affects the transport properties of electrons in the inversion layers in bulk Si MOS structures, resulting in significant lowering the electron mobility as compared to its value in the bulk Si. It is reasonable to expect that due to the presence of two Si/SiO_2 interfaces and different carrier distributions in the Si layer, the behavior of the electron mobility in SOI inversion layers should differ from that in bulk Si inversion layers. For this reason, the electron mobility in SOI MOSFETs has been extensively studied both experimentally [130-133, 164] and theoretically [165-170]. Main attention was paid to the influence of Si film thickness and the comparison of mobilities in single-gate and double-gate structures.

5.5.1. Mobility in single-gate SOI MOSFETs

Experimental studies have shown that in the case of SOI devices with sufficiently thick Si films ($t_{Si} \geq 50$ nm), the carrier mobility in the inversion layer does not depend on the Si film thickness and is similar to that in bulk structures. However, starting from a certain value ($t_{Si} \approx 15\ldots20$ nm), with decreasing the Si film thickness, sharp degradation of the effective electron mobility is observed, which is most pronounced in the region of low carrier densities or transverse effective fields [130-133, 164].

It has been shown that there are several factors resulting in reduction of the effective electron mobility in ultra-thin SOI devices with decreasing t_{Si}. These factors are enhancement of surface roughness scattering and Coulomb scattering by interface charges caused by approaching of charge carriers to the interface, as well as enhancement of interaction of charge carriers with non-uniformities and interface charges at the back Si film/buried SiO_2 interface [164, 167-169]. Another factor is enhancement of the carrier confinement in the transverse direction with decreasing t_{Si}, which increases the phonon-scattering rate and thereby decreases the carrier mobility [165-167]. In addition, ultra-thin SOI MOS structures feature enhanced scattering by surface optical phonons as compared to that in bulk Si MOS structures due to the presence of two Si/SiO_2 interfaces, and this scattering mechanism is very sensitive to the thickness of the Si film [169]. The role of these factors is strongly dependent on the carrier density in the Si film. Based on the analysis of the experimental and theoretical data, it has been concluded that strong reduction of the electron mobility with decreasing the Si film thickness, which is observed in the range of low electron densities, is mainly caused by enhancement of phonon scattering and Coulomb scattering by interface charges.

5.5.2. Mobility in double-gate SOI MOSFETs

The carrier mobility in DG SOI MOSFETs has been studied in many theoretical works [166, 169-171]. It has been shown that the effective carrier mobility in DG SOI MOSFETs is strongly influenced by the effect of *volume inversion*. Volume inversion weakens the main scattering mechanisms (*i.e.*, phonon scattering, surface roughness scattering, and Coulomb scattering by interface charges), which provides an increase in the effective carrier mobility. The weakening of Coulomb scattering by interface charges and surface roughness scattering in the volume inversion regime is explained by the fact that spreading of charge carriers over the Si film thickness

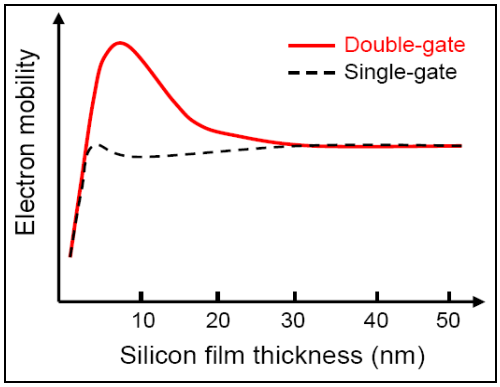

Fig. 22. Qualitative representation of the effective electron mobility variation with the Si film thickness in double-gate and single-gate SOI MOSFETs predicted by theoretical studies [170].

moves the charge centroid further away from the interface [169-171]. The weakening of the phonon scattering in the volume inversion mode results from reduction of the carrier confinement in the transverse direction [166, 169, 170]. Due to the volume inversion effect, the effective carrier mobility in DG SOI devices may exceed the mobility in single-gate SOI devices and bulk Si devices at the same values of the effective transverse electric field or carrier densities. In DG SOI structures with very thin silicon films, as in single-gate SOI structures, the geometric factor is decisive. Behavior of the effective electron mobility in double-gate and single-gate SOI MOSFETs with variation of t_{Si} predicted by theoretical studies is schematically shown in Fig. 22.

In Fig. 22, three regions of t_{Si} with different mobility behavior can be distinguished. In the region of thick Si films, for which there is no interaction between two inversion channels, the mobility in double-gate and single-gate SOI MOS structures is the same. The second region corresponds to the range of t_{Si}, where in DG SOI devices there is interaction between both inversion layers, and where the volume inversion effect occurs. The value of t_{Si}, at which the transition to this region occurs, strongly depends on the value of the transverse effective field (or inversion charge density), because at high transverse electric fields or carrier densities, a potential barrier is formed in the middle of the film, which reduces the overlap of two inversion channels (see Fig. 21). In this region of intermediate values of t_{Si}, the effective mobility in double-gate SOI MOS structures increases with decreasing t_{Si} and is higher than in single-gate structures, due to the volume inversion effect. Finally, in the region of very thin Si films (t_{Si} < 10 nm), where the geometric factor becomes decisive, the mobility in both types of structures sharply decreases with decreasing t_{Si}. From the foregoing, it follows that behavior and magnitude of the effective carrier mobility in double-gate SOI MOSFETs can differ significantly from those in counterpart single-gate SOI MOSFETs and bulk Si MOSFETs.

6. Conclusions

SOI offers many advantages over bulk Si technology, especially for fabrication of CMOS ICs. Below, we have summarized the key benefits of SOI CMOS devices:

- ⇒ *excellent radiation hardness to transient radiation effects and high-energy particles* due to elimination of latch-up effect and greatly reduced charge collection volume;
- ⇒ *capability of operation at high temperatures;*
- ⇒ *higher operation speed* due to reduced parasitic and junction capacitances resulting from the presence of buried oxide and the use of the thin Si film;
- ⇒ *reduction of undesirable short-channel effects* achievable by using the thin-film and multiple-gate MOSFET architectures, which enables to continue the MOSFET shrinking into the nanometer region;
- ⇒ *the ability to lower the operation voltage and dramatically reduce energy consumption* due to steeper subthreshold characteristics, feasibility to use a lower threshold voltage, and reduced charging/discharging capacitance.

Owing to these properties, SOI has now become leading technology for manufacturing ultra-large-scale ICs for a wide range of applications. In addition to its traditional applications in radiation-hardened and high-temperature electronics, SOI is presently used for manufacturing mainstream electronic components, namely: high-speed microprocessors, memory chips, RF chips, microcontrollers for portable and mobile electronic devices, wireless communication systems, *etc*., which take advantage of high speed, low-voltage operation and low power consumption of SOI devices. Furthermore, the role of SOI is growing when going from microelectronics to nanoelectronics.

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Розвиток приладів типу «кремній-на-ізоляторі» (КНІ) та їх основні властивості

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Анотація. Кремній-на-ізоляторі (КНІ) є найбільш перспективною кремнієвою технологією на сьогоднішній день. Використання технології КНІ забезпечує значні переваги порівняно з традиційною технологією об'ємного кремнію при виготовленні багатьох типів інтегральних схем (ІС), зокрема, комплементарних метал-оксид-напівпровідник (КМОН) ІС. Технологія КНІ також дозволяє подальшу мініатюризацію КМОН-приладів у нанометровому діапазоні. У цьому огляді коротко описано еволюцію технології КНІ та її основні області застосування. Представлено основні технологічні методи виготовлення пластин КНІ. Описано принципові переваги КНІ-приладів порівняно з приладами на об'ємному кремнії. Розглянуто типи КНІ метал-оксид-напівпровідникових (МОН) транзисторів і їх основні електричні властивості.

Ключові слова: кремній-на-ізоляторі (КНІ), метал-оксид-напівпровідник (МОН) транзистор, КНІ-транзистори з багатостороннім затвором, КНІ-транзистор з надтонкою кремнієвою плівкою, повністю збіднений КНІ-транзистор, зарядовий зв'язок меж поділу.