Semiconductor Physics, Quantum Electronics & Optoelectronics, 2021. V. 24, No 3. P. 277-287.

Physics of microelectronic devices

Measuring of an unknown voltage by using single electron transistor based voltmeter

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Abstract. In engineering and science, high operating speed, low power consumption, and high integration density equipment are financially indispensable. Single electron device (SED) is one such equipment. SEDs are capable of controlling the transport of only one electron through the tunneling transistor. It is single electron that is sufficient to store information in SED. Power consumed in the single electron circuit is very low in comparison with CMOS circuits. The processing speed of single electron transistor (SET) based device will be nearly close to electronic speed. SET attracts the researchers, scientists or technologists to design and implement large scale circuits for the sake of the consumption of ultra-low power and its small size. All the incidences for the case of a SET-based circuit happen when only a single electron tunnels through the transistors under the proper applied bias voltage and a small gate voltage or multiple gate voltages. For implementing a single electron transistor based voltmeter circuit, SET would be the best candidate to fulfil the requirements of it. Ultra-low noise is generated during tunneling SEDs. A D Flip-Flop is implemented and based on this, two kinds of registers like sequence register and code register are made.

Keywords: electron tunneling, Coulomb blockade, single electron transistor, successive approximation register.

https://doi.org/10.15407/spqeo24.03.277
PACS 07.50.Ek, 74.55.+v, 84.30.-r, 85.30.Mn, 85.30.Tv, 85.40.-e

Manuscript received 18.03.21; revised version received 16.06.21; accepted for publication 18.08.21; published online 26.08.21.

1. Introduction

Civilization of mankind is advancing step-by-step in every developing field for human benefit. It has been conferred incalculable benefit to the human society from technological end. Now civilized mankind is at the door of more advanced and sophisticated technology that it can get the desired result within a pico- to nanosecond, *i.e.*, in order of 10^{-18} to 10^{-15} s. The more mankind is getting successes, the more its responsibility is increasing for inventing more unknown things. The tremendous desire for invention of new things causes it to encounter the challenges in the competitive world of engineering and technology. In nano- and pico-electronics, one of the challenges is to develop and integrate VLSI based on a new paradigm for digital processing. For getting so, one must first look for or create a device which can perform the logic operation in such a way that is completely different from the way they are implemented by ordinary BJT or CMOS. An approach to these new devices can be built on the basis of the concept of single electron tunneling under the control of proper small bias and input voltages. The fundamental component of any logic gates, combinational as well as sequential circuits is called the single electron transistor [1–3]. Depending upon the tunneling mode and Coulomb blockade, the name of a gate is designated.

In this work, an inverter, a 3-input NAND gate and a sequential circuit acting as D Flip-Flop are implemented. Having combined with them, two types of registers are built. And finally, a control logic successive approximation register is presented as a prime functional unit in our present work – single electron transistor based voltmeter.

2. Coulomb blockade and single electron transistor

A tunnel junction consisting of a thin insulating barrier between the two conducting electrodes is shown in Fig. 1a. The electrodes in this tunnel junction may be superconducting or semiconducting if they become superconducting, electrons with one elementary charge (1.602×10^{-19} C) carry the current.

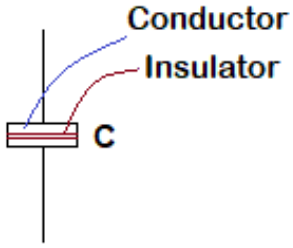

Fig. 1a. Tunnel junction.

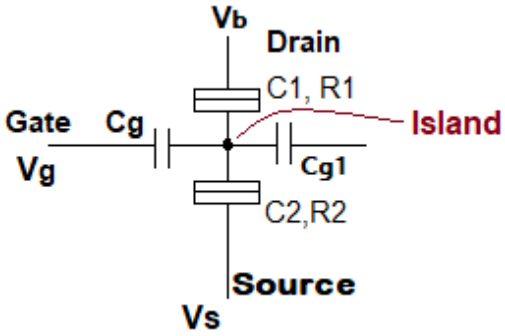

Fig. 1b. Single electron transistor (SET).

In classical electrodynamics, current can't flow through an insulating barrier. But in the case of quantum mechanics, there must be a non-disappearing (*i.e.*, more than zero) probability for an electron residing one side of the barrier to reach the other side of it. If proper bias voltage is applied, there will be a current flow. Neglecting additional effects, in accordance with first-order–approximation-tunneling, current is proportional to the applied bias voltage. In the case of electrical terms, a tunnel junction behaves as a resistor having a constant value depending on the barrier thickness. If two conductors are connected with an insulating layer between them, there will have not only a resistance but also a capacitance. In this context, the tunnel junction acts as a capacitor and the insulator as dielectric. For the discrete nature of electric charge, current flowing through a tunnel junction is a series of events in which merely one electron can pass or tunnel through the tunnel junction. As the single electron tunnels through the junction, the tunnel capacitance is charged with an elementary charge (1.602×10^{-19} C) building up a voltage $V = e/C$, where C is the junction capacitance. When the capacitance of the tunnel junction is drastically small, the voltage built up in the tunnel junction may be adequate to prevent another electron to tunnel. The electrical current is suppressed then as the bias voltage is lower than the voltage created in the tunnel junction, and the resistance of the device will no longer remain constant. The increment of the differential resistance of the tunnel junction around zero bias is called the Coulomb blockade [3, 4].

The principle of single electronics [4–6] is developed on the basis of the Coulomb blockade and single electron tunneling. Single electron tunneling circuits appear to be a promising candidate for future VLSI circuits for its ultra-low power consumption, ultra-small size, reducing node capability and rich functionality. A single electron transistor (SET) [4, 5] with two tunnel junctions shown in Fig. 1b having capacitances and resistances C_1, C_2 and R_1, R_2, respectively, shares only a common island with a low capacitance. The electric potential of the island can be tuned by a third electrode, called gate, which is capacitively coupled (gate capacitance C_g) to the island. An extra capacitance C_{g1} may intentionally be connected to the island for the purpose of adjusting the gate (input) voltage. The drain, source and gate voltages are indicated by V_b, V_s and V_g, respectively. For proper operations of SET both of the resistances R_1 and R_2, are to be greater than $Rq = h/e^2 \approx 25.8\,\text{k}\Omega$, and charging energy $E_C = e^2/2C$ ($C = C_1 + C_2 + C_g + C_{g1}$) has to be greater than thermal fluctuations kT, *i.e.*, $E_C = e^2/2C > kT$, the product of the Boltzmann constant k and the temperature T. The Boltzmann constant value is 1.380649×10^{-23} J/K or 1.380649×10^{-16} erg /K.

3. Inverter

The inverter [7–10] depicted in Fig. 2a is constructed with two single SETs in series connection. Input voltage is directly coupled to the islands of SET1 and SET2 through two capacitors C_1 and C_2, respectively. The island of each SET is a very small piece of gold having total capacitance C_{tot} = 1pF. The two extra gates V_{g1} and V_{g2} are intentionally connected to the islands of SET1 and SET2 through two capacitors C_{g1} and C_{g2}, respectively,

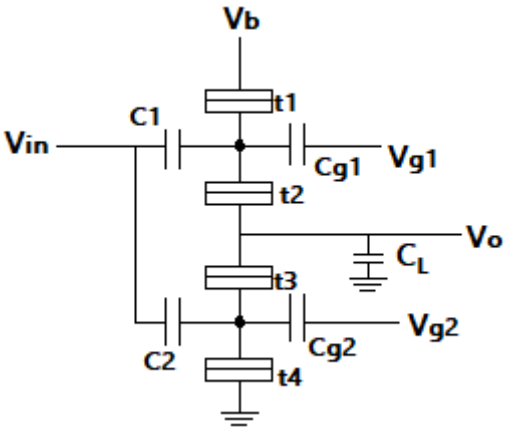

Fig. 2a. Inverter.

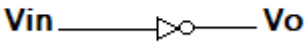

Fig. 2b. Symbol of an inverter.

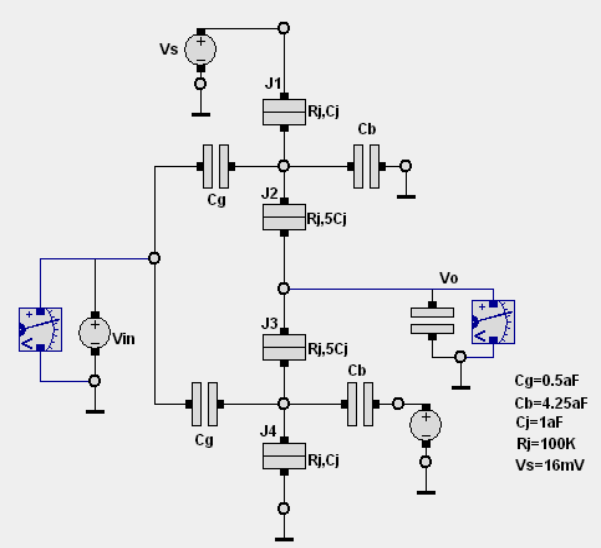

Fig. 2c. Simulation set of inverter.

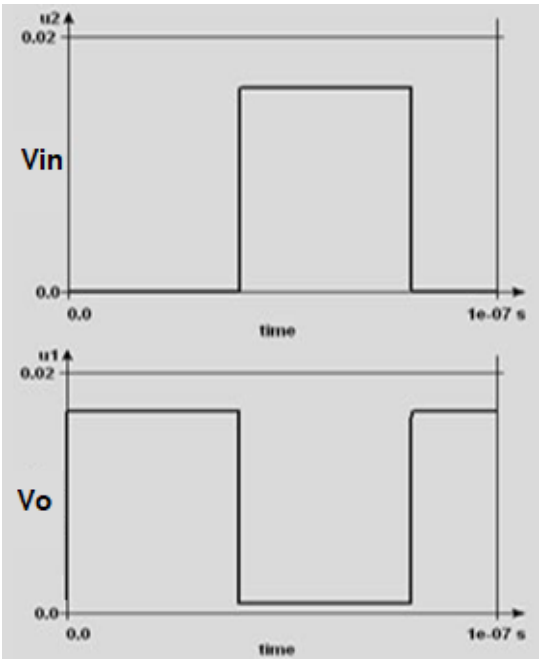

Fig. 2d. Simulation result of inverter.

to tune the induced charges on the islands of SET1 and SET2. The output terminal V_0 is connected to the common channel of the two SETs and to the ground *via* a capacitor C_L to put down charging effects.

For the case of inverter, the parameters values chosen are: $V_{g2} = 0$, $V_{g2} = 0.1q_e/C$, $C_L = 9C$, $t_4 = \frac{1}{10}C$, $t_3 = \frac{1}{2}C$, $t_2 = \frac{1}{2}C$, $t_1 = \frac{1}{10}C$, $C_1 = \frac{1}{2}C$, $C_2 = \frac{1}{2}C$, $C_{g1} = \frac{17}{4}C$ and $C_{g2} = \frac{17}{4}C$, $R_1 = R_2 = 100$ kΩ. For the simulation cases the value of C, as we consider, is 1 aF.

The operation of the inverter will be like this: the output V_0 value will be high when the input voltage V_{in} is low, and V_0 value will be low when the input voltage is high. For achieving this target, the applied bias voltage $V_{g1} = 0$ and $V_{g2} = 16$ mV along with the tuning gate voltages (at present V_{in}) of SET1 and SET2 are provided. Now, if V_{in} is low, the SET1 is in conduction mode and the SET2 is in Coulomb blockade.

This effectively results the output to voltage V_b and causes the output voltage to high, *i.e.*, this effectively connects the output to the supply voltage and makes the output high. Coulomb blockade interferes the steady flow of current as when the high voltage is applied to the input it causes to shift the induced charge on each of the islands of these two SETs by a fraction of an electron charge and keeps the SET1 in Coulomb blockade and SET2 in conducting mode. As a result, the output shifts from high to low.

In this work, we assume the Boolean logic inputs corresponding to the voltages like: logic "0" = 0 V and logic "1" = $0.1q_e/C$.

We assume, for simulation and other purposes, $C = 1$ aF then logic "1" = $0.1\frac{1.602\cdot10^{-19}}{1\cdot10^{-18}}0.1$ = $0.1\cdot1.602\cdot10^{-2} = 16.02\cdot10^{-3}$ $16.02 \cong 16$ mV.

4. Single electron transistor based 3-input NAND gate

By using six single electron transistors (SETs), a 3-input NAND gate [2, 3, 11, 12] can be constructed as depicted in Fig. 3a. SET circuits are configured as CMOS circuits, the pull up transistor (upper three parallel transistors) called *p*-channel (P-SET) is tied to V_d and the pull down transistor (lower three transistors connected in series) called *n*-channel transistor (N-SET) tied to ground. The *p*-channel has thrice the area factor of the *n*-channel SET, which is equivalent to setting thrice the gate width.

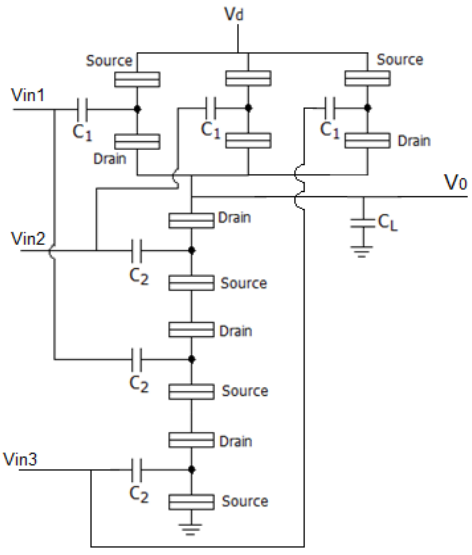

Fig. 3a. 3-input NAND gate.

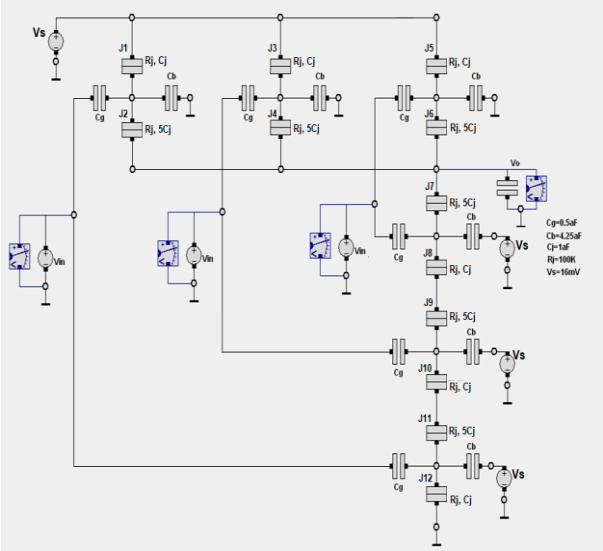

Fig. 3b. Simulation set of 3-input NAND.

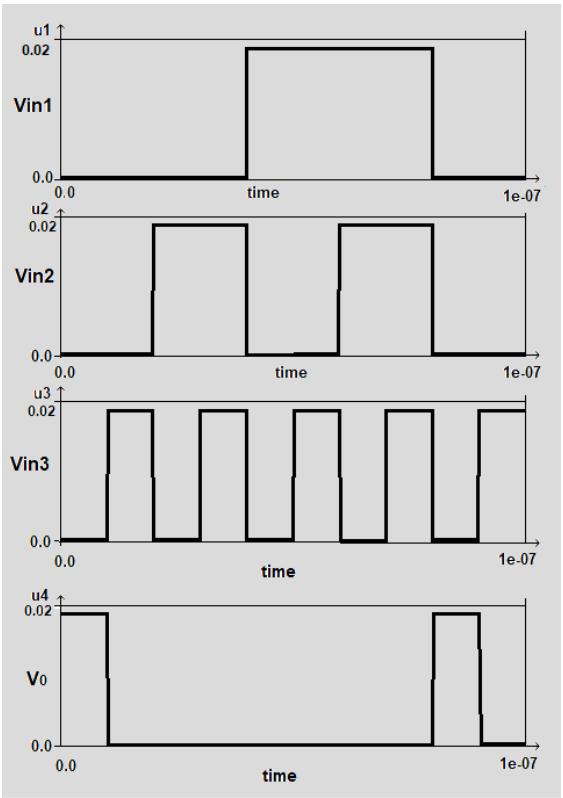

Fig. 3c. Simulation result of 3-input NAND.

For the case of SET 3-input NAND gate, the upper three SETs called *p*-channel SETs (P-SETs) are connected in parallel and the lower three SETs called *n*-channel SETs (N-SETs) are connected in series. When these both input voltages V_{in1}, V_{in2} and V_{in3} are high, the lower three SETs are in tunneling mode, and single electron is passing through them and virtually the output V_0 connected to ground which leads to low value. On the other hand, if anyone or both of the inputs V_{in1}, V_{in2} and V_{in3} are low, N-SETs are in Coulomb blockade and the output is pulled to V_d by P-SETs, which (either one or both) are in tunneling mode and the resultant output becomes high [13, 14].

To simulate the 3-input NAND gate, the parameters values chosen are: C_L = 9 aF, Drain = 0.5 aF, Source = = 0.5 aF, $C_1 = C_2 = 0.5$ aF, $C_{g1} = C_{g1} = \frac{17}{4}C = 4.25$ aF, $R_1 = R_2$ = 100 kΩ, high logic voltage is 16 mV and low logic 0 V. The simulation result is shown in Fig. 3c.

5. Implementation of a D Flip-Flop

Using the tunneling phenomenon for the case of SETs and the setting pattern of them, we will be able to implement of a universal NAND gate [4, 5, 7, 14] and based on that any combinational as well as sequential gate/circuit can be constructed. We are interested in constructing a D Flip-Flop with the help of a 3-input NAND gate shown in Fig. 3a as well as Fig. 3b. In quest of a D Flip-Flop having the input side as "Set", "CLK", "Data" & "Reset" and the output side as Q and $\bar{Q}$, anybody can set six 3-input NAND gates [15, 16] in the pattern shown in Fig. 4 to create a D Flip-Flop. The result of this Flip-Flop is provided in Table 1.

The truth table given in Table 1, we have assumed a Trigger Condition = 0 to 1, which represents a rising edge clocked Flip-Flop; Set/Reset level in our case = 1.

6. Successive approximation type analog-to-digital

Successive approximation type analog-to-digital converter (ADC) is widely used in multi-meter, voltmeter and popular ADC method. The conversion time is kept constant in this type of ADC method, and is proportional to the length of word, *i.e.*, how many output bits from MSB to LSB in the digital output, unlike the counter and continuous type A/D converters. The basic principle of this type of ADC is being that the unknown analog input voltage to be measured is approximated against a 5-bit digital value, in this paper, by trying one bit at a time, commencing with the most significant bit. The successive approximation process for a 5-bit conversion is explained here. This type of analog-to-digital conversion is operated by successively dividing the voltage range by 2, as explained in the following steps.

Table 1.

Inputs				Outputs	
D	CLK	Set	Reset	Q	$\bar{Q}$
0	↑0	0	0	0	1
1	↑0	0	0	1	0
0 or 1	↑0	1	0	1	0
0 or 1	↑0	0	1	0	1
0 or 1	↑1	1	1	Last Q	Last $\bar{Q}$

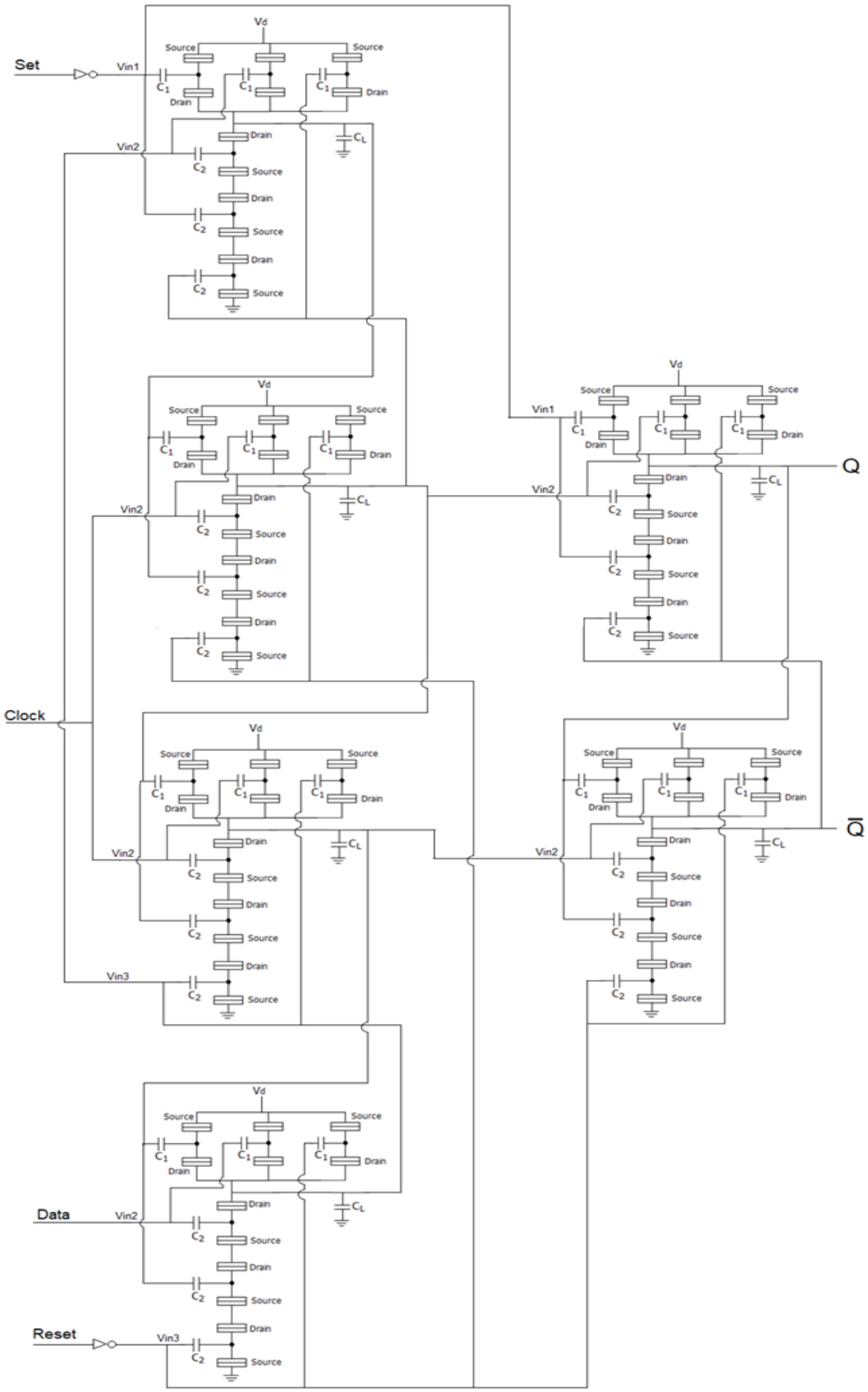

Fig. 4. SET based D Flip-Flop.

At the getting started, (1) MSB is initially set to 1, *i.e.*, the first register (FF1) output level for a five-bit register is unity with the remaining four bits set as 0000. The digital equivalent voltage V_D ($10000_2 = 16_{10}$) is now compared with the unknown analog input voltage. (2) If the analog input voltage is higher than the digital equivalent voltage 16_{10}, MSB is kept the same as 1 and the second MSB (4^{th} bit from LSB) is set to 1 otherwise, MSB is set to 0 and the second MSB (4^{th} bit from LSB) is set to 1. In both cases, either the unknown voltage is higher or lower than the reference voltage, one must set the second MSB 1. Comparison is made according to step 1 to decide whether to retain or reset the second MSB and so on.

The above steps can be illustrated using the following example. Let us assume that the 5-bit ADC is used, and the analog input voltage is $V_A = 9.5$ mV. At the time of getting started conversion, the MSB bit is set to 1. We have taken the scaling factor = 2, so the scaled value of 9.5 is equal to $2 \cdot 9.5 = 19$.

Now $V_A = 19 > V_D = 16 = [10000]_2$. Here, the unknown input voltage $V_A = 19$ is higher than the digital voltage V_D, as described in the step 2, MSB will be kept the same as 1 and the next MSB bit will be set to 1 as follows: $V_D = 24$ V $= [11000]_2$.

Now $V_A = 19 < V_D = 24 = [11000]_2$. Here now, the unknown analog input voltage V_A is lower than the equivalent digital voltage V_D. As discussed in the step 2, the second MSB is set to 0 and next MSB set to 1 as $V_D = [10100]_2 = 20$.

Now again $V_A = 19 < V_D = 20 = [10100]_2$. Like to that discussed in the step 2 $V_A < V_D$, hence the third MSB is set to 0 and the 4^{th} MSB bit is set to 1. The new code word is $V_D = 18 = [10010]_2$.

Now again $V_A = 19 > V_D = 18$ V $= [10010]_2$. The unknown input voltage $V_A = 19$ is higher than the equivalent digital voltage V_D, as discussed in the step 2 above, MSB should be kept the same as 1 and the next MSB bit, here it is LSB, of course, is set to 1. $V_D = 19 = [10011]_2$. $V_A = 19 = [10011]_2$.

Table 2.

5-bit word	Eqvt. Voltage (mV)	5-bit word	Eqvt. Voltage (mV)
00000	0	10000	8.0
00001	0.5	10001	8.5
00010	1.0	10010	9.0
00011	1.5	10011	9.5
00100	2.0	10100	10.0
00101	2.5	10101	10.5
00110	3.0	10110	11.0
00111	3.5	10111	11.5
01000	4.0	11000	12.0
01001	4.5	11001	12.5
01010	5.0	11010	13.0
01011	5.5	11011	13.5
01100	6.0	11100	14.0
01101	6.5	11101	14.5
01110	7.0	11110	15.0
01111	7.5	11111	15.5

Now finally, $V_A = V_D$, conversion stops. So, the value of the unknown voltage $= [10011]_2 = 19$ (scaled value).

And its real value is equal to $\frac{19}{2} = 9.5$ mV .

This unknown value measurement process is depicted in Table 2.

$$\frac{5 \text{ bit value}}{32} \times (\text{Ref. } V)$$

$$\text{Eqvt. Volt.} = \frac{16}{32} \times (5 \text{ bit value}) = 0.5 \times (5 \text{ bit value})$$

We assume that the analog voltage is 9.5 V, then we obtain the output bit word (10011) from the above discussion. The process is pictorially represented in Fig. 5.

The unknown input, reference voltage value, different stages of comparisons and the final digital output of five bits are shown in the binary tree in Fig. 6. Any of the values in the leaf stages of the tree can be obtained against the root value by Fig. 6 after the time duration between start-of-conversion (SOC) and the end of the conversion (EOC).

7. Voltmeter

The main part of the architecture of voltmeter is the "control logic SAR" unit, which consists of two parts: (i) sequence register and (ii) code register. The code register acts as control logic. The combined form of (i) and (ii) parts is referred to as the successive approximation register (SAR) [17]. SAR is operative to determine the value of each bit in a sequential manner, in accordance with the output coming from comparator. SAR gets started the conversion cycle by putting the most significant bit, MSB, of the word, equal to 1, keeping all the other bits of the word equal to 0. The word created, *i.e.*, 10000 is applied to the digital-to-analog converter (DAC) which converts the digital word into analog value, that is one half the conversion range, *i.e.* $V_{ref}/2$. This value is now compared to the unknown input voltage V_{in} to be measured.

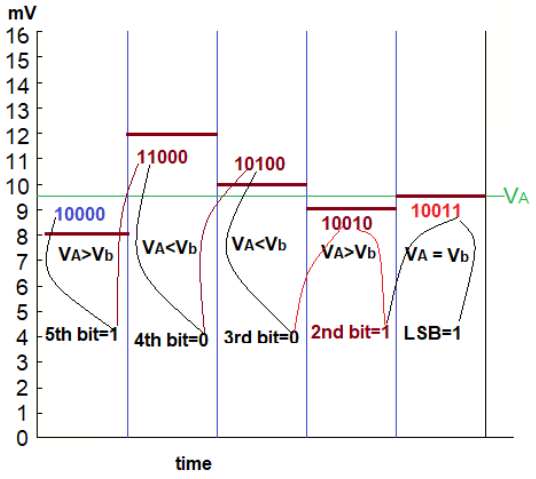

Fig. 5. Graphical representation of evaluation of digital value.

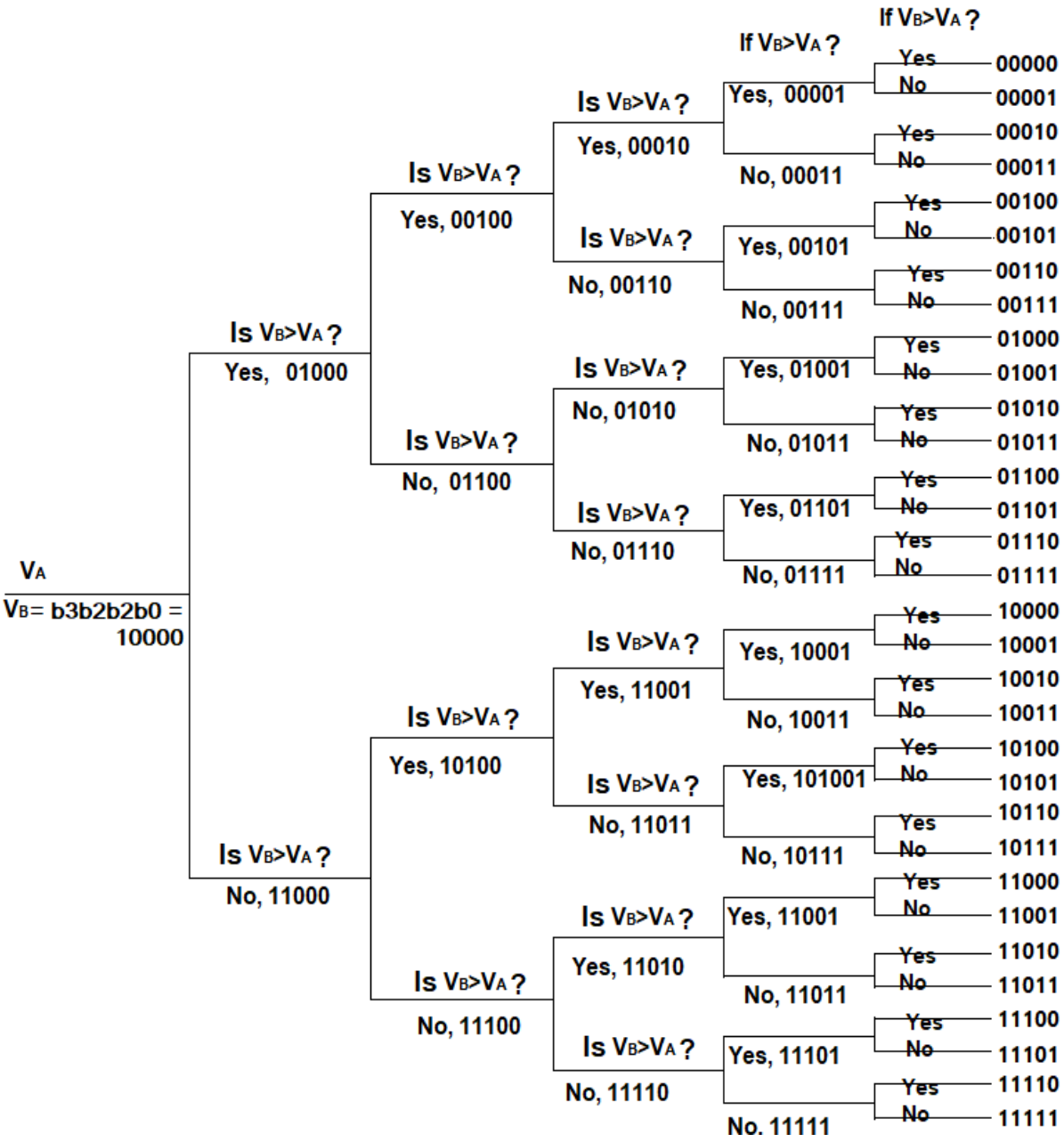

Fig. 6. Conversion sequence of 5-bit successive approximation A/D.

The operation of SAR is as follows.

At the beginning, we connect the RST input to the 0 input level, and it controls the SET input (Fig. 7) of the 1st Flip-Flop (FF1) of the sequence register and RESET inputs of all the remaining sequence registers Flip-Flops. The same RST bus also controls the RESET inputs of code register Flip-Flops (CFFs). The outputs of Q and $\overline{Q}$ of the 1st Flip-Flop (FF1) are set to 0 and 1, respectively. The output of $\overline{Q}$ controls the SET input of the first Flip-Flop (CFF1) of the code register. As a result, the output of CFF1 is enforced to 1. This enforced 1 will be the most significant bit (MSB) of the code register and will be the weight, while the full scale range of voltage is $V_{ref}/2$.

As the sequence register is reset at first, the set line of all the code registers Flip-Flops is at logic 0 unlike CFF1. So, all the other code register outputs, of course, are at logic 0. Hence, MSB of the code register becomes 1, and all others are at logic 0 s. DAC will generate the corresponding weighted analog equivalent voltage. This analog quantity is delivered to one input port of comparator. The other input terminal of the comparator is connected with sampled V_{in} of the unknown voltage. The comparator output is now (d_4), which is either 1 or 0.

At the time when the RST input goes high and clock is triggered positively, the output Q of FF1 becomes 0 (Table 1). As is shown from Fig. 7, the D input of FF1 register array is set to ground and second Flip-Flop (FF2)

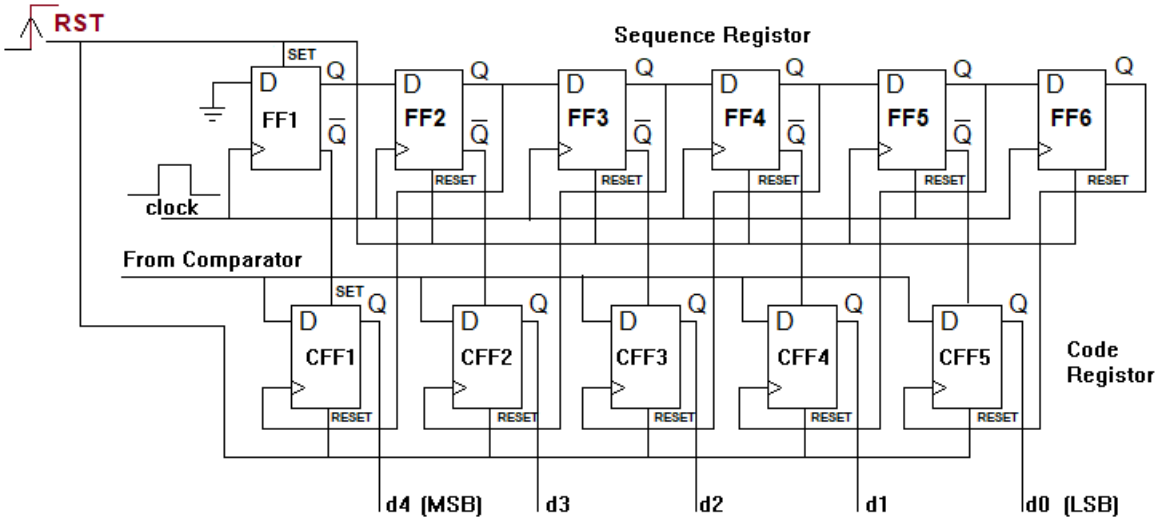

Fig. 7. Control logic SAR.

output logic becomes 1 (as RESET is high so FF2's logic value equals 1). The low level to high level transition of FF2 definitely triggers 1st Flip-Flop (CFF1) of the code register to store control bus value d_4 of the comparator output to CFF1. Till now, when the clock signal runs further, the code register Flip-Flop retains the set value as FF2 output goes to zero.

The same procedure is followed for each of Flip-Flops, until after 5-clock cycles a high logic, *i.e.*, 1 comes out of last sequence Flip-Flop FF6, which controls the least significant bit (LSB) of the code register. After 5-clock cycles, end-of-operation is finished, and the digital output is shown at the screen of the LED/seven-segment display (Fig. 7a).

8. Control logic SAR

The contents of the control logic SAR register represent the digital outcome shown by the LED/seven-segment display of the completed conversion. This SAR consists of a sequential registers and code registers providing finite-state machine (FSM) that generates the sequence of states shown in the following Table 3 (wherein the case of the number of bits being $i = 5$ has been considered, for simplicity).

The sequence unfolds as follows: in step 1, the initializing configuration is enforced with a value 1. Over the following steps, three actions are possible on the single bit: enforcement of the attempt 1, result of the decision from the comparator and memory of the preceding value.

For the case of a successive approximation algorithm, one can describe Table 3 by the following. Initial step MSB bit = 1, and remaining 4-bits are 0 s. This bit word is converted into analog value by DAC and is being passed through the comparator for comparing with an unknown voltage. The output signal from comparator is d_4.

Step 1:
This d_4 is kept in MSB position (2nd row in Table 3) and the second MSB position is filled with 1 and the rest positions by 0 s. The word [d_4 1000] is passed through DAC and comparator as done in initial step, and we get the output signal from comparator as d_3.

Step 2: The two bits d_4 and d_3 are kept in MSB and 2nd MSB positions and the 3rd MSB is set to 1, the remaining two positions are filled with two 0 s. Now the word [d_4 d_3 100] is passed through DAC and comparator as done in initial step, and we get the output signal from comparator as d_2.

Step 3: The three bits d_4, d_3 and d_2 are kept in MSB, 2nd MSB and 3rdMSB positions and the 4th MSB is set to 1, the remaining one position is filled with one 0. Now the word [d_4, d_3 d_2 10] is passed through DAC and comparator as done in the previous step(s), and we get the output signal from comparator as d_1.

Step 4: The four bits d_4, d_3, d_2 and d_1 are kept in MSB, 2nd MSB, 3rd MSB and 4th MSB positions and the 5th MSB, which is now LSB is set to 1. Now the word [d_4 d_3 d_2 d_1 1] is passed through DAC and comparator as done in the previous step(s), and we get the output signal from comparator as d_0.

Step 5: The last signal d_0 coming from comparator is set to LSB position. Processing is completed, and we will get the binary output [d_4 d_3 d_2 d_1 d_0].

Table 3.

Conversion step	Digital-to-analog input word					Output of comparator
1	1	0	0	0	0	d_4
2	d_4	1	0	0	0	d_3
3	d_4	d_3	1	0	0	d_2
4	d_4	d_3	d_2	1	0	d_1
5	d_4	d_3	d_2	d_1	1	d_0
Result	d_4	d_3	d_2	d_1	d_0	–

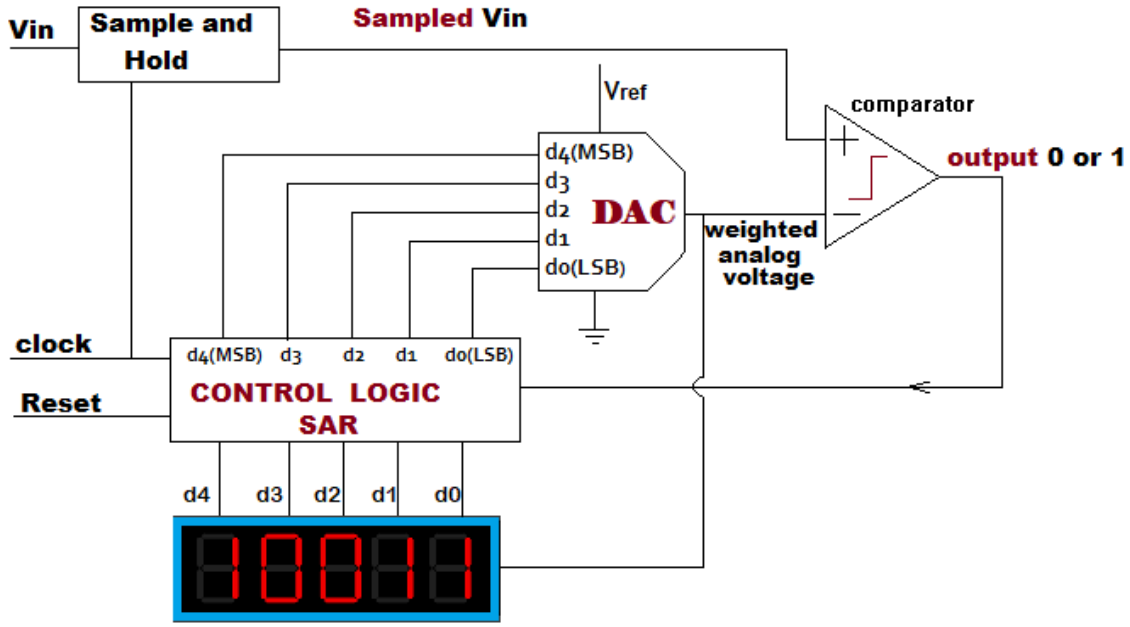

Fig. 7a. Voltmeter.

This word [d_4 d_3 d_2 d_1 d_0] of 5 bits is the digital value of the input unknown voltage, which we can get from the logic control SAR shown in Fig. 7a.

9. Time delay

For a CMOS/TTL logic gate the time delay/processing delay for a gate like NAND, NOR, XOR is 12 ns [7, 18], on the contrary the time required for tunneling through a SET is approximately 4 ns [4, 5]. The XOR gate using conventional logic circuits needs 16 transistors, whereas this function can be implemented with just one SET [2, 4–6], *i.e.*, no. of nodes are reduced to 1 instead of 16.

All the gates and devices drawn in Fig. 1 through 3 are combinational. Fig. 4 is sequential. The inverter consisting of two SETs takes 8 ns for tunneling. The three input NAND gate is made up of six SETs, it requires total tunneling time 16 ns, since upper three SETs need only 4 ns for tunneling, and lower three SETs need $3 \times 4 = 12$ ns. D Flip-Flop implemented requires $16 \times 2 = 32$ ns for the same purpose. The time it requires for control logic SAR drawn in Fig. 8 to tunnel is $(32 \times 2) \times 6 = 384$ ns, *i.e.*, time duration between start-of-conversion and end-of-conversion is 64 ns. Table 4 provides us the tunneling times for different components. Graphical representation of Table 4 is shown in Fig. 8.

From Table 4, we can find the output rate for control logic SAR is $\frac{1}{384\,\text{ns}} = \frac{10^9}{384} = 2604167$ Hz.

Table 4.

Circuit name	SET Circuit delay (ns)
Inverter	$4 \times 2 = 8$
3-input NAND	$4 \times 4 = 16$
SET	$4 \times 1 = 4$
XOR	$4 \times 1 = 4$
D Flip-Flop	$16 \times 2 = 32$
Single step for SAR	$32 \times 2 = 64$
SAR	$32 \times 2 \times 6 = 384$

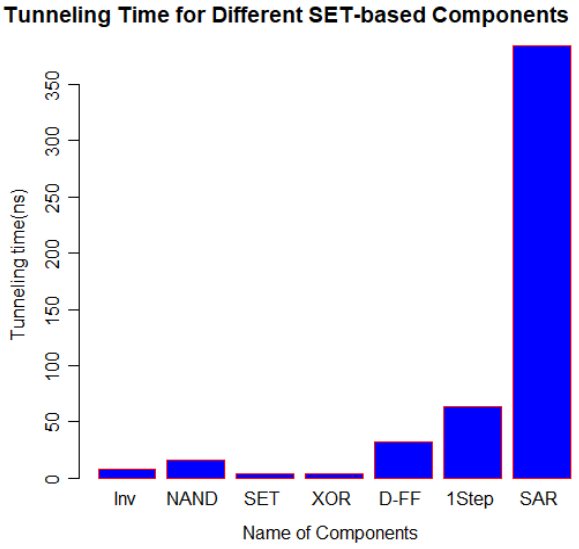

Fig. 8. Tunneling time *vs* components.

10. Switching energy

For switching energies required for AND, OR, NOR, NAND and Inverter are 10.8, 10.8, 10.7, 10.7, and 10.4 meV, respectively [19]. Depending on these, the switching energies necessary for the 3-inpur NAND gate, D Flip-Flop and square SAR circuit in this work are given in Table 5. It is really clear that the energy required will be of order O (10^{-18}). So, very negligible energy is required in comparison with our conventional TTL-, JFET- or CMOS-based gates O (10^{-6}). Table 5 values are represented by the graphical representation given in Fig. 9.

Some relevant comparison between CMOS and SET are also attached in Table 6 [16].

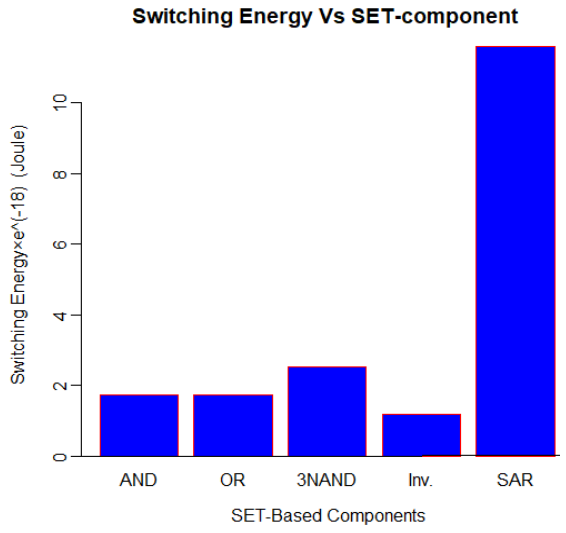

Fig. 9. Switching energy *vs* components.

Table 5.

Gate name	Required elements	Energy (Joules)
AND	thirteen (13)	1.73016 e^{-18}
OR	thirteen (13)	1.73016 e^{-18}
3-input NAND	nineteen (19)	2.52869 e^{-18}
Inverter	nine (9)	1.197803 e^{-18}
SAR	eighty seven (87)	11.578763 e^{-18}

Table 6.

	CMOS circuit	SET circuit
Switching speed	10^{-10} s	10^{-15} s
Operating temperature	> 300 K	< 300 K
Current range	nA	electrons
Voltage range	100 mV	16 mV

11. Conclusions

In this work, we have elaborately discussed concerning control logic SAR with two sets of registers: the sequence and code ones. The digital-to-analog converter is not discussed here separately. DAC is made up of a ladder resistor circuit and an amplifier. Both the sequence and code registers are made up of registers that are also implemented with D Flip-Flops made up of single electron transistors. As to SED based voltmeter, we have implemented it as consisting of three parts: (i) digital word controlling part, (ii) digital-to-analog converter and (iii) comparator. After properly connecting them, the unknown voltage ranging between 0 and 16 mV can be measured in the digital word of five bits. We have studied the time delays both for CMOS/TTL logic and SET based logic and found that SET related circuit at least 3 times faster than CMOS/TTL based classical logic. The switching power in the case of SET based devices are of the order of O (10^{-17}), which is very low. Single electron-based devices have turned out to be valuable tools in the research of science and engineering fields. They have drawn one's attention as the SET-devices that consume very low power and require a small number of nodes, which provides higher order integrity of population (*i.e.*, large-scale integration) and gives the output rate much better than O (10^{-6}).

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Вимірювання невідомої напруги за допомогою вольтметра на основі одноелектронного транзистора

A.K. Biswas

Анотація. У науці та техніці висока робоча швидкість, низьке споживання енергії та обладнання з високою щільністю інтеграції є фінансово необхідними. Одноелектронний пристрій – приклад такого обладнання. Одноелектронні пристрої здатні контролювати перенесення лише одного електрона крізь тунельний транзистор. Саме одного електрона вистачить для зберігання інформації в одноелектронному пристрої. Потужність, яка споживається в єдиному електронному ланцюзі, є дуже низькою у порівнянні зі схемами CMOS. Швидкість обробки пристрою на основі одноелектронного транзистора буде майже наближена до швидкості електрона. Використання одноелектронного транзистора залучає дослідників, вчених або технологів до проектування та реалізації великомасштабних схем задля споживання наднизької потужності та її малих розмірів. Усі процеси у схемі на основі одноелектронного транзистора відбуваються, коли тільки один електрон тунелює крізь транзистори під належною напругою зміщення та малою напругою затвора або підвищеною напругою затвора. Для реалізації єдиної схеми вольтметра на основі одноелектронного транзистора, одноелектронний транзистор буде найкращим кандидатом для виконання таких вимог. Під час тунелювання в одноелектронному пристрої генерується наднизький рівень шуму. Реалізовано D Flip-Flop, і на основі цього створюються два типи регістрів, такі як регістр послідовностей та регістр коду.

Ключові слова: тунелювання електрона, кулонівська блокада, одноелектронний транзистор, регістр послідовного наближення.