Semiconductor Physics, Quantum Electronics & Optoelectronics, 2022. V. 25, No 3. P. 289-293.

Hetero- and low-dimensional structures

The peculiarity of capacitance-voltage characteristics of the metal-insulator-nanowire structure

S.G. Petrosyan, S.R. Nersesyan

Institute of Radiophysics and Electronics, NAS of Armenia, 0203 Ashtarak, Armenia
E-mail: stepan.petrosyan@rau.am

Abstract. The quasi-static capacitance-voltage characteristics of the metal-insulator-nanowire structure have been theoretically studied with account of the surface states at the nanowire-insulator interface. At small radii, possible is the case when the entire bulk of nanowire is depleted before the onset of inversion of the conduction type near the surface will occur. In this case, there is a strong deviation of the capacitance-voltage characteristic from that in the standard MIS structure: with increasing voltage, the capacitance of the structure tends not to a constant value equal to the capacitance of the dielectric layer, but to zero.

Keywords: nanowire, capacitance, surface states, MIS structure.

https://doi.org/10.15407/spqeo25.03.289
PACS 62.33.Hj, 73.03.-b, 85.30.Kk

Manuscript received 07.05.22; revised version received 14.06.22; accepted for publication 21.09.22; published online 06.10.22.

1. Introduction

Devices based on semiconductor nanowires (NWRs) are of great interest for many applications, including diodes and transistors [1–3], solar cells [4], capacitors [5], photo-detectors [6], *etc*. The cylindrical geometry of the NWR makes it attractive to create a field-effect transistor with a metal gate covering the channel from all sides (gate-all-around or wrap-gate), which provides better electrostatic control of the channel conductivity than in the usual planar structure [7]. Operation of such a transistor is based on the structure of a metal-insulator-NWR, the longitudinal conductivity of which is controlled by the voltage on the surrounding metal electrode.

Due to the cylindrical geometry and finiteness of the NWR radius, formation of depletion and inversion layers and, accordingly, the capacitive characteristics of metal-insulator-semiconductor (MIS) structures acquire new features and phenomena that are absent in planar structures can be observed.

This becomes especially evident when the radius of the depletion region becomes comparable to the radius of NWR, and the entire bulk of NWR is covered by the space charge (SC). Depending on the radius and doping level of NWR, a situation can arise when an inversion layer cannot appear near the surface at all, which should radically change the capacitance-voltage characteristic of these MIS structures.

The purpose of this work was to study the features of capacitance inherent to MIS structures based on NWRs of different diameters, taking into account the surface states (SS) at the NWR-insulator interface. In this work, we will consider the low-frequency capacitance, when the period of the measuring signal is longer than the lifetime of minority carriers, and the charge in the inversion layer and on the SS have time to follow the changes in the gate voltage.

2. Model and calculation results

Let us consider the structure of a metal-insulator-semiconductor NWR. At the center of the structure, there is a semiconductor NWR (for example, from *n*-Si) of radius R, with a uniform donor concentration N_D (all donors are considered to be ionized). Silicon NWR is coated with an insulator layer of thickness d (for example, SiO_2), with the dielectric constant ε_D, onto which a thin layer of a metal gate is deposited.

For simplicity of calculations, let us consider the case of the so-called ideal MIS structure, when it is assumed that the thermodynamic work functions of the semiconductor and metal coincide, there are no charged centers in the bulk of the insulator, and the resistance of the gate insulator is infinitely large (the thickness is so large that there is no through tunnel current).

It is well known that, both on the free surface of a semiconductor and at the interface with an insulator, there are usually SS that are quasi-continuously distributed over the band gap of the semiconductor [8–10]. According to their charge state, SS can be of both acceptor and donor types. Usually, acceptor-type SSs are located in the upper half of the band gap, and donor-type SS are located in the lower half. To take into account the effects associated with SS, we will assume that SS with a constant density N_{SS} are distributed over the entire band gap of NWR.

The presence of SS at the semiconductor-insulator interface leads to the fact that before application of an external voltage, the energy bands are bent. Since we are considering *n*-type NWR, acceptor-type SS are first filled, therefore, the energy bands are bent upwards, a region of positive SC of width *W* (depletion region) is formed in the semiconductor, and a potential barrier is formed for electrons near the surface of NWR.

If an external negative voltage is applied, the metal will be charged negatively, the energy bands bending will increase. A further increase in the external negative voltage can lead to such band bending that donor SS will also become activated.

Without entering into the details of barrier potential formation, let us suppose that the surface potential of NWR (more precisely, the potential energy of electron) is given and equal to U_S. As usual, U_S will be related to the gate voltage.

Within the framework of depletion layer approximation, the Poisson equation for the electrostatic potential energy of electrons $U(r)$ in the SC region $(R-W \le r \le R)$ in cylindrical coordinates is written as:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dU(r)}{dr}\right)=\frac{e\rho(r)}{\varepsilon_S\varepsilon_0}, \quad (1)$$

where e is the absolute value of the electronic charge, ρ is the volume charge density, ε_S is the dielectric constant of the semiconductor, ε_0 is the electrical constant. At depleting voltages, assuming that the charge in the SC region is positive and generally consists of the charge of ionized donors and free holes in the inversion layer (neglecting the mobile electrons in the SC region), we can write the following expression for $\rho(r)$:

$$\rho(r)=e\left(N_D+\frac{n_i^2}{N_D}\exp\left[\frac{U(r)}{kT}\right]\right), \quad (2)$$

where n_i is the intrinsic concentration of charge carriers, k is the Boltzmann constant and T is the absolute temperature. Using (2), the equation (1) can be reduced to the dimensionless form:

$$\frac{1}{x}\frac{d}{dx}\left(x\frac{dy}{dx}\right)=A(1+B\exp[y]), \quad (3)$$

where $x\equiv\frac{r}{R}$, $y\equiv\frac{U}{kT}$, $A\equiv\frac{R^2}{L_E^2}$, $L_E^2\equiv\frac{\varepsilon_S\varepsilon_0 kT}{e^2N_D}$, $B\equiv\frac{n_i^2}{N_D^2}$.

Boundary conditions in our case reflect the absence of an electric field at the SC region edge, as well as the choice of the potential reference point:

$$\begin{cases} y'(1-z)=0 \\ y(1-z)=0 \end{cases} \quad (4)$$

where $z\equiv\frac{W}{R}$.

During the numerical solution of the Poisson equation in the region of $(1-z \le x \le 1)$ for the given gate potential, the surface potential can be considered as an additional condition for finding the depletion region width *W*, assuming that on the NWR surface $U(R) = U_S$, *i.e.*,

$$y(1)=y_S. \quad (5)$$

The electrical neutrality equation for our structure has the form:

$$Q_M+Q_{SC}+Q_{SS}=0, \quad (6)$$

where Q_M is the charge on metal ($Q_M < 0$), Q_{SC} is SC ($Q_{SC} > 0$), Q_{SS} is the surface charge (all these charges are considered per unit length of NWR). Expressing these charges *via* the surface potential y_S and surface electrical field y'_S, we will come to the equation that for the given gate potential must be satisfied at the actual value of depletion width *W*.

The charge of SS Q_{SS} can be expressed in terms of the surface band bending,

$$Q_{SS}=-2\pi ReN_{SS}(U_0-U_S)=-2\pi RekTN_{SS}(y_0-y_S), \quad (7)$$

where $U_0=kT\ln\frac{N_D}{n_i}$ is the energy distance from the Fermi level to the middle of the band gap in the quasi-neutral region of NWR.

In general, the given external potential φ_G (surrounding gate potential) and the surface potential φ_S of semiconductor are related by the equality

$$\varphi_G-\varphi_G=\frac{Q_M}{C_{OX}}, \quad (8)$$

where C_{OX} is the capacitance of the dielectric layer per unit length of NWR. It is well known that

$$C_{OX}=\frac{2\pi\varepsilon_D\varepsilon_0}{\ln\left[\frac{R+d}{R}\right]}. \quad (9)$$

Using (6), the equation (8) can be written in the form

$$y_G-y_S=\frac{e(Q_{SC}+Q_{SS})}{kTC_{OX}}. \quad (10)$$

Integrating the equation (3) and using the boundary conditions (4), we get for SC:

$$Q_{SC}=2\pi e N_D L_E^2 y'_S. \quad (11)$$

Finally, substituting (7) and (11) into (10), we obtain an equation relating the surface potential and electric field of NWR

$$y_G-y_S=\frac{2\pi\varepsilon_S\varepsilon_0}{C_{OX}}y'_S-\frac{2\pi Re^2N_{SS}}{C_{OX}}R(y_0-y_S). \quad (12)$$

We can say that, in fact, we have replaced the condition (5) with the new relation (12).

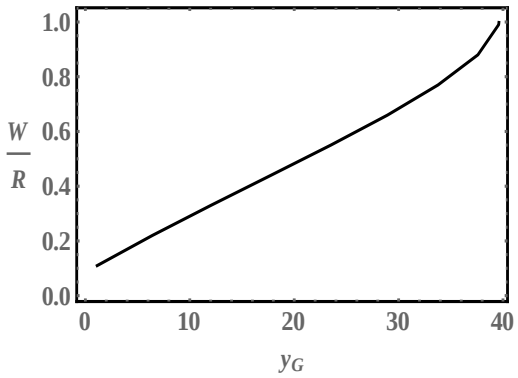

Fig. 1. Dependence of the depletion layer thickness on the applied voltage for NWR with R = 50 nm.

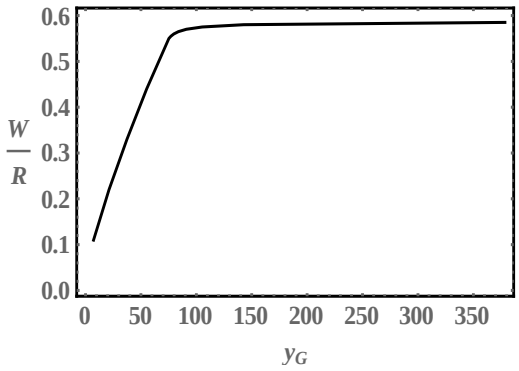

Fig. 2. Dependence of the depletion layer thickness on the applied voltage for NWR with R = 100 nm.

Now, by numerically solving the Poisson equation (3) with the boundary conditions (4) and taking into account the relation (12), we can find the dependence of the surface potential y_S and the width of depletion region on the gate voltage y_G, *i.e.*, on the magnitude of the external voltage applied between the metal and NWR.

For brevity, we present only the dependence of the depletion region width on the external voltage. Assuming $N_D = 5\cdot10^{17}$ cm^{-2}, $N_{SS} = 5\cdot10^{11}$ cm$^{-2}\cdot$eV^{-1}, $d =$ 10 nm and for clarity, we consider two cases of the NWR radius: R = 50 nm (Fig. 1) and R = 100 nm (Fig. 2).

It can be seen from Fig. 1 that at R = 50 nm, with an increase in the external voltage, the depletion region gradually expands and completely covers the bulk of NWR. This is the case when the band bending in NWR is insufficient for the inversion of the conduction type near the surface. When R = 100 nm (Fig. 2), we have a completely different picture: starting from a certain value of the external voltage, the transition between depletion and strong inversion occurs, after which the SC region practically does not expand. In this case, SC is mainly due to the charge of holes in the inversion layer, the value of which increases logarithmically with increasing the gate voltage.

It is of interest to study the capacitance-voltage characteristics of the structure under consideration. When the voltage on the metal electrode changes, the SS charge changes, therefore, these states have a certain capacitance and, in turn, affect the distribution of the applied voltage between the space charge region of the semiconductor and the insulator layer.

Naturally, the presence of SS and a change in their charging state will also affect the capacitance-voltage characteristic of the metal-insulator-NWR structure.

In general, the capacitance C of the structure, by definition, is equal to

$$C = \left|\frac{dQ_M}{d\varphi_G}\right|. \tag{13}$$

Using (8), the equation (13) can be represented as

$$\frac{C}{C_{OX}} = 1 - \frac{dy_S}{dy_G}. \tag{14}$$

Knowing the dependence of the surface potential on the external voltage ($y_S(y_G)$), it is easy to find a capacitance-voltage characteristics. We present the results of numerical calculations for NWs of three different diameters: 50 (Fig. 3), 80 and 100 nm (Fig. 4).

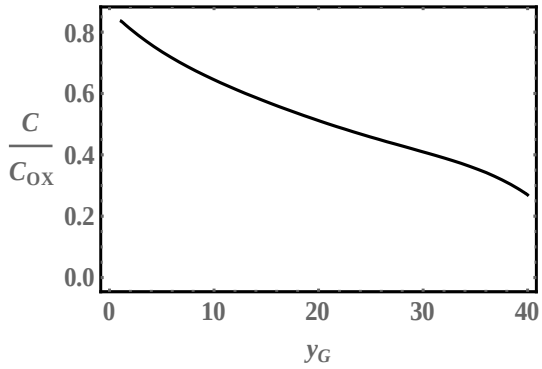

Fig. 3. Gate voltage dependence of the structure capacitance for the NWR radius R = 50 nm.

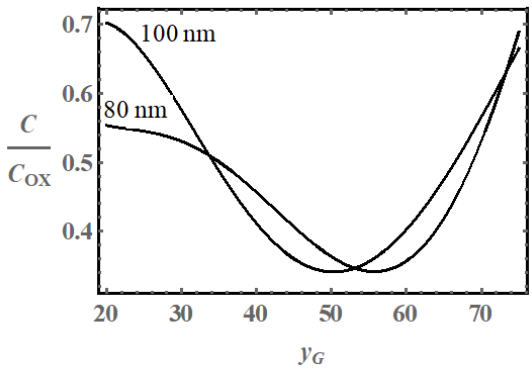

Fig. 4. Gate voltage dependence of the structure capacitance for the NWR radii R = 80 and 100 nm.

As noted above, at R = 50 nm, NWR is completely depleted before the onset of inversion, and with increasing external voltage, the capacitance of the structure tends to zero (in the case of the standard MIS structure, it should tend to C_{OX}). At R = 80 and 100 nm, the situation changes: starting from a certain moment, an inversion occurs near the NWR surface, the capacitance of structure begins to grow and tends to a constant equal to the capacitance of the dielectric layer C_{OX} .

These features in behaviour of the capacitance-voltage characteristic for the metal-insulator-NWR structure were observed in many experimental works [5, 9, 11, 12], and the obtained above theoretical results are in qualitative agreement with the experimental data.

Analyzing the adduced above, it can be argued that at a given doping level and density of surface states, there is a certain critical radius R_C, below which NWR is completely depleted before the onset of inversion, *i.e*., an inversion layer does not appear in NWR at large depleting voltages.

In full depletion layer approximation, the relationship between the surface potential $\varphi_S = -\frac{U_S}{e}$ and the depletion layer width can be obtained from (1) by ignoring in the right hand the space charge of free holes and using the same boundary conditions (4):

$$\varphi_S = \frac{eN_D R^2}{2\varepsilon_S \varepsilon_0}\left[\frac{(R-W)^2}{2R^2} - \frac{1}{2} - \frac{(R-W)^2}{R^2}\ln\frac{R-W}{R}\right]. \quad (15)$$

Using this equation and taking into account the condition of the inversion layer appearance near the surface, when $W \to R$, at $\varphi_S \to -\frac{2U_0}{e}$, one can obtain

$$R_C = \sqrt{\frac{8\varepsilon_S \varepsilon_0 kT}{e^2 N_D}\ln\frac{N_D}{n_i}} \quad . \quad (16)$$

Estimating the value of critical radius for the considered parameters of NWR, we get R_C = 67 nm. Note that we found approximately this value in exact numerical calculations.

We noted above that the presence of SS, in turn, affects the capacitance-voltage characteristics of the metal-insulator-NWR structure. To demonstrate the influence of this factor, let us compare the capacitance-voltage characteristic of the structure in the presence of SS and in their absence. The calculated capacitance-voltage characteristics of this structure for NWR with R = 50 and 80 nm are presented in Figs 5 and 6, respectively.

As it follows from Figs 5 and 6 in the general case, the presence of surface states does not change the qualitative form of the capacitance-voltage characteristics, but only leads to a quantitative shift of these characteristics.

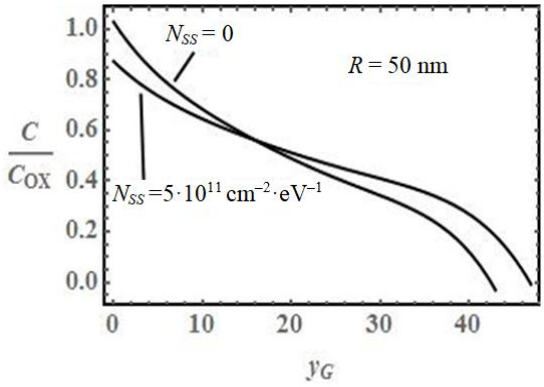

Fig. 5. Capacitance-voltage characteristics of MIS structure for the NWR radius R = 50 nm in the presence and absence of SS.

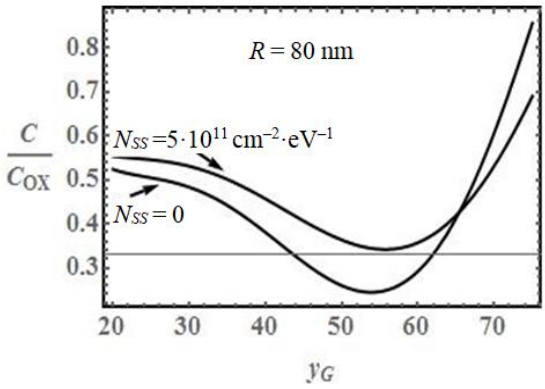

Fig. 6. Capacitance-voltage characteristics of MIS structure for the NWR radius R = 80 nm in the presence and absence of SS.

3. Conclusions

In this work, we have considered the features of the low-frequency capacitance-voltage characteristics of an ideal metal-insulator-nanowire structure with account of surface states at the nanowire-insulator interface. At small NWR radii, when an external depleting voltage is applied to the metal gate, the NWR bulk can be completely covered by the space charge before the inversion occurs. In this case, the capacitance-voltage characteristics are significantly different from those in the case of a standard MIS structure. As the voltage increases, the capacitance of the structure tends not to a constant value, as usual equal to the capacitance of the insulator layer, but to zero.

Conflict of interest

The authors declare no conflict of interest.

References

1. Singh B., Prasad B. and Kumar D. Silicon nanowire parameter extraction using DFT and comparative performance analysis of Si NWFET and CNTFET devices. *Semiconductors*. 2021. **55**. P. 100–107. https://doi.org/10.1134/S1063782621010152.

2. Borblik V.L. Electrostatics of the nanowire radial *p-i-n* diode. *SPQEO*. 2019. **22**. P. 201–205. https://doi.org/10.15407/spqeo22.02.201.
3. Zhu H. Semiconductor nanowire MOSFETs and applications. In: *Nanowires – New Insights*. M. Khan (Ed.). IntechOpen: London, UK, 2017. https://doi.org/10.5772/67446.
4. Otnes G., Borgström M.T. Towards high efficiency nanowire solar cells. *Nano Today*. 2017. **12**. P. 31–45. https://doi.org/10.1016/j.nantod.2016.10.007.
5. Hourdakis E., Casanova A., Larrieu G., Nassiopoulou A.G. Three-dimensional vertical Si nanowire MOS capacitor model structure for the study of electrical versus geometrical Si nanowire characteristics. *Solid State Electron*. 2018. **143**. P. 77–82. https://doi.org/10.1016/j.sse.2017.11.003.
6. Petrosyan S., Yesayan A., Nersesyan S. Photo-current relaxations and gain in semiconductor nano-wires. *Proc. SPIE*. 2014. **94400**. P. 94400R-1–9. https://doi.org/10.1117/12.2180885.
7. Sze S.M., Li Y., Ng Kwok K. *Physics of Semi-conductor Devices. 4th Edition.* Wiley, NY, 2021.
8. Xu Q., Y. Dan Y. Uncovering the density of nanowire surface trap states hidden in the transient photoconductance. *Nanoscale*. 2016. **8**. P. 15934–15938. https://doi.org/10.1039/C6NR05014J.
9. Garnett E., Tseng Yu-C, Khanal D. *et al*. Dopant profiling and surface analysis of silicon nanowires using capacitance–voltage measurements. *Nature Nanotechnology*. 2009. **4**. P. 311–314. https://doi.org/10.1038/nnano.2009.43.
10. Gurwitz R., Shalish I. Method for electrical characterization of nanowires. *Nanotechnology*. 2011. **22**. P. 435705–435707. https://doi.org/ 10.1088/0957-4484/22/43/435705.
11. Leontis I., Botzakaki M.A., Georga S.N., Nassiopoulou A.G. High capacitance density MIS capacitor using Si nanowires by MACE and ALD alumina dielectric. *J. Appl. Phys*. 2016. **119**. P. 244508-1–6. https://doi.org/10.1063/1.4954883.
12. Karlström O., Wacker A., Nilsson K. *et al*. Analyzing the capacitance–voltage measurements of vertical wrapped-gated nanowires. *Nanotechnology*. 2008. **19**. P. 435201–435207. https://doi.org/10.1088/0957-4484/19/43/435201.

Authors and CV

Stepan G. Petrosyan, Professor, the corresponding member of NAS of Armenia, the head of Laboratory of Semiconductor Nanoelectronics at the Institute of Radiophysics and Electronics of NAS of Armenia, born in 1951. He defended PhD thesis in 1977 and Doctor of Sciences thesis in Physics and Mathematics (Semiconductor Physics) in 1990 at the Vilnius State University and Sankt-Peterburg Polytechnical University, correspondingly. He is authored over 130 publications, 6 patents, 5 monographs and textbooks. The area of his scientific interests includes physics and technology of semiconductors, heterostructures, two-dimensional crystals, quantum dot and nanowires devices (thin film solar cells, photodetectors, FET, *etc*.).
https://orcid.org/0000-0003-1746-7005

Suren R. Nersesyan,
Researcher at the Laboratory of Semiconductor Nanoelectronics in the Institute of Radiophysics and Electronics, NAS of Armenia, born in 1987. He defended PhD thesis in Physics and Mathematics (Semiconductor Physics) in 2013 at the Yerevan State University, Armenia. Authored over 10 publications. The area of his scientific interests includes theory of semiconductor devices and low-dimensional heterostructures.
E-mail:suro10@rambler.ru,
https://orcid.org/0000-0003-0622-5326

Authors' contributions

Petrosyan S.G.: conceptualization, methodology, writing – original draft, review & editing.
Nersesyan S.R.: software, visualization, writing – original draft.

Особливості вольт-фарадної характеристики структури метал-ізолятор-нанодріт

С.Г. Петросян, С.Р. Нерсесян

Анотація. Теоретично досліджено квазістатичні вольт-фарадні характеристики структури метал-ізолятор-нанодріт з урахуванням поверхневих станів на межі нанодріт-ізолятор. При малих радіусах можливий випадок, коли весь об'єм нанодроту виснажується до початку інверсії типу провідності біля поверхні. При цьому спостерігається сильне відхилення вольт-фарадної характеристики від такої в стандартній структурі метал-ізолятор-нанодріт: зі збільшенням напруги ємність структури прямує не до постійного значення, який дорівнює ємності шару діелектрика, а до нуля.

Ключові слова: нанодріт, ємність, поверхневі стани, структура метал-ізолятор-нанодріт.