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Production of GaAs transistors with the Schottky barrier in Bi-GaAs-$AsCl_3$-HCl-$SnCl_2$-H_2-He system by epitaxial deposition

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Abstract. Investigation results in the preparation technology of perfect GaAs structures doped with Sn and Bi in the GaAs-Bi-$AsCl_3$-HCl-H_2-He system by the isothermal chloride epitaxy method has been presented. A complex problem has been solved to obtain planar layers of i-n^0-n-n^+ type field-effect transistors with the Schottky barrier. Preparation of planar active layers of these transistors with electron concentration in the active layer $N_e = 3\cdot10^{17}$ cm^{-3}, mobility μ = 4300 cm^2/V·s (T = 20 ºC) has been described. The growth regime of GaAs doped with Sn and Bi in the scheme with "competing etching" has been found at the temperature 700 °C in the precipitation zone onset and the temperature gradient −2ºC/cm. The optimum parameters of structure growth were presented and discussed. This allowed to create the discrete field-effect transistors with the Schottky barrier with improved operating characteristics on their basis. The current-voltage characteristics of individual devices obtained in one technological cycle were within the range of 20 to 21 mA/V.

Keywords: GaAs field-effect transistor, Schottky barrier, CVC.

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The progress in the development of semiconductor devices for microwave engineering, including field-effect transistors with the Schottky barrier (FTSB) and digital big integrated circuits (BIC) on the basis of these devices, is associated with the gallium arsenide use [1]. However, to make a practical use of those advantages, it is necessary to solve a complex of problems concerning the optimization of device design philosophy, taking into account the technical means of their production which are much different from those of silicon-based devices.

The gas-phase epitaxy (GPE) in the chloride or chloride-hydride systems is a method of promise to produce GaAs FTSB structures [1, 2]. These epitaxial methods allow to grow layers GaAs with micron and submicron thickness d, active n-layer at the concentration $N_e = (1…5)\cdot10^{17}$ cm^{-3} as well as to obtain the whole i-n^0-n-n^+ FTSB structure using a single production process (Fig. 1).

The BICs on the basis of field transistors with the Schottky barrier made on the basis of i-n^0-n-n^+ structure (Fig. 1) have unstable electrophysical characteristics and a low reproduction of parameters over the plate surface. Such deterioration of electrophysical characteristics results from the mutual diffusion of the buffer n^0 layer alloying components with the active n-layer. Additional electron levels that spread to the active area are formed near the interface of n^0- and n-layers. Diffusion leads to the emergence of short- and long-term drift mechanisms. The reason for the parameters spreading over the active epitaxial layer grown is the uneven distribution of the dislocation density over the substrate. Thus, the low device structure perfection and the insufficiently uniform density of defects and uncontrolled dopants over the substrate surface area are the main factors hindering the development of this technology.

The work [3] deals with possible mechanisms of dislocation density reduction in the active n-layer. It has been shown that to create 3-4 layer structures, the type and concentration of dopant in a substrate and layer as well as the number of layers and their arrangement in the structure should be taken into account. To reduce the negative effect of the substrate, buffer layers were used, the type and parameters of which determine the electron mobility value and the level of their compensation in the active layer, and in the final analysis, the current-voltage characteristic (CVC) slope, FTSB noise, and frequency characteristics and their stability [1].

A basic trend of the epitaxial growth is to reduce the temperature and to use the isothermal regime of growing $A^{III}B^V$ compounds [4, 5]. This results from the

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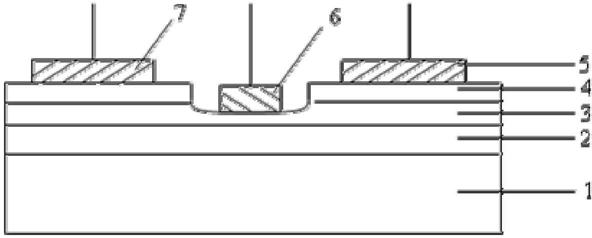

Fig. 1. Scheme of field-effect transistor with the Schottky barrier: 1 – AGChPK-type substrate (GaAs:Cr), d = 350 μm; 2 – buffer n^0-layer (GaAs), d = 3 μm, $N_e < 10^{15}$ cm^{-3}; 3 – active n-layer (GaAs:Sn:Bi), d = 0.2 μm, $N_e = 3\times10^{17}$ cm^{-3}; 4 – contact n^+-layer (GaAs:Sn), d = 2 μm, $N_e = 3\times10^{18}$ cm^{-3}; 5 – drain Au+Ge/Ni; 6 – gate Au+Ge/Ni; 7 – source Au+Ge/Ni.

epitaxy temperature reduction causing an increase in microuniformity of the layer grown due to the reduction of dopant diffusivity and intrinsic point defects, for which the dislocations serve as an effective getter [6].

The buffer n^o-layer of major area is grown by the GPE method in order to reduce and equalize the density of dislocations over the entire surface area of GaAs:Cr substrate (Fig. 1), 10^5 to 10^3 cm^{-3} from the center to periphery and the concentration of point defects and deep or shallow acceptor uncontrolled dopants (Cr, Fe, Mn, and other) [7], diffusing during the growth from substrate to the active n-layer. To make the buffer n^0-layer, we used the low-temperature growth method (that we have developed [8]), which allows to grow the buffer n^0-layer 2-3 μm thick of pure GaAs during a single processing cycle of a uniflow horizontal reactor. By itself, the buffer layer consists of thin sublayers 0.15 μm thick of pure GaAs with various concentrations of deep EL_2 levels. This deformed buffer layer allows to effectively getter the uncontrolled dopants and electrically active defects of substrate, thus preventing them from diffusing into the active n^0-layer. The biggest heterogeneity of the n^0-layer growth rate can be observed at first 1.5…2 cm of GaAs deposition area in the GaAs-$AsCl_3$-H_2 subsystem (Fig. 2). In this area, the uncontrolled dopants implanted into n^0-layer enter into the gas phase from the GaAs solid source. It should be emphasized that silicon is the basic uncontrolled dopant entering into the active n-layer (GaAs:Sn) from the gas phase [9]. Silicon is formed in the n-layer due to formation of $SiCl_3$ or SiCl in the gas phase, depending on the temperature condition of the active n^0-layer growth. The $SiCl_3$ or SiCl molecular compounds are formed as a result of undercutting of (SiO_2) HCl quartz reactor walls, thus being a source of Si in the n-layer.

It was shown in the work [10] that in GaAs and GaP bulk crystals this reduction of silicon uncontrolled dopant concentration was detected due to isoelectronic doping, the concentration of Si in GaAs decreasing in the course of isoelectronic doping with Sb-In-Bi dopants [10]. In this connection, we have investigated the gas phase formation in the GaAs-Bi-$AsCl_3$-HCl-H_2-He system [11] to obtain the source of Bi growth in GaAs in the form of $BiCl_3$ at low growth temperatures of 670 to 720 ºC. It was shown that when Bi interacted with $AsCl_3$ in He in the Bi-$AsCl_3$ subsystem, $BiCl_3$ became saturated at the temperature of 600 to 620 ºC, while in the Bi-HCl-H_2 subsystem $BiCl_3$ became saturated at the temperature of 800 to 830 ºC. This fact allows to assert that the Bi-$AsCl_3$-He and GaAs-$AsCl_3$-H_2 subsystems of the GaAs-Bi-$AsCl_3$-HCl-H_2-He system can be used separately in one of the multichannel reactor channels described in [12] with the purpose of the gas phase formation at the low-temperature isothermal growth of GaAs doped with Bi.

To prepare the active n-layer of FTSB structure, the growth temperature regime and the gas phase composition in the GaAs-Bi-$AsCl_3$-HCl-H_2-He system were optimized. The minimum scatter in thin tin and bismuth doped layers thickness (about 2 %) is observed within a narrow interval of $AsCl_3$ molar concentrations (from $5\cdot10^{-4}$ to $2\cdot10^{-3}$) at the fixed growth temperature equal to 700 ºC. The formation of highly uniform GaAs:Sn:Bi films can be explained by that, in the above-mentioned growth regime, the rates of atomic components implanting into the growing layer structure become comparable with their mass transfer rate. To attain a more uniform doping of the active layer by tin than that reported in [13], we have used an additional introduction of HCl-H_2 into the growth zone under a slight negative gradient of the substrate temperature, $\Delta T/x = -2$ ºC/cm. $BiCl_3$-He, doping GaAs with Bi isovalent dopant, was introduced through another additional channel into the growth zone. Since the tin and bismuth contribution coefficient between the gas phase and GaAs is proportional to HCl concentration, the rate of the gas phase depletion in $SnCl_2$ and $BiCl_3$ is about four times reduced at the constant growth temperature due to three-fold decrease of the growth rate at the point $x = 0$ (the forward substrate butt end) and the simultaneous increase of HCl concentration in the gas phase. This allowed to prepare reproducibly active n-layers uniform in thickness and dopant content with a mobility of 4300 cm^2/V·s (at 22 ºC) and charge carrier concentration of $3\cdot10^{17}$ cm^{-3}.

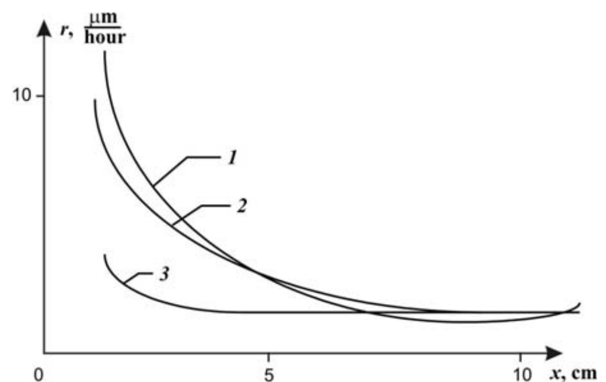

Fig. 2. Change in GaAs growth rate along substrate for various gas phase compositions at the reactor inlet. The total concentration of α chlorides: 1 – 0.9 %, 2 – 0.55, 3 – 0.1.

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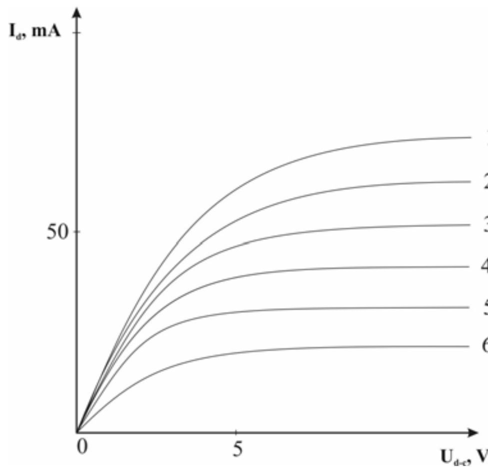

Fig. 3. Output CVC of GaAs field-effect transistor with the Schottky barrier in common drain scheme: U_{s-g} = 0 (1); –1 V (2); –2 (3); –3 (4); –4 (5); –5 (6).

Parameters of the subcontact layer do not necessarily meet the requirement of a high doping uniformity in the structure plane, because, once the contact resistivity is lowered down to (1…5)·10^4 Ohm·cm, the further decrease in the source and drain resistance becomes indecisive on the background of the passive resistance of the FTSB channel. A tin concentration in gallium arsenide about 10^{18} cm^{-2} is sufficient to assure the required contact resistivity between n^+-contact layer and Au+Ge/Ni ohmic contact. To deposit the subcontact layer with an electron concentration of such value, the partial pressure of $AsCl_3$ being introduced into the tin supply was increased up to 2.3×10^{-2} molar parts, thus allowing to obtain the above-mentioned parameters. The epitaxial structures obtained on 40 mm dia. substrates were used to prepare low-power FTSB with the gate width 1.5 μm and distance between the source and drain 5 μm on the operating area of 30×40 mm^2. The voltage on the transistor gate corresponding to the complete channel cutoff was determined at the gate-source voltage U_{g-s} = – 4 V. The FTSB characteristic slope was measured at the drain-source U_{d-s} = 2 V. Fig. 3 shows the set of CVC for the transistors under study. The FTSB CVC slope values prepared in one procedure cycle in the GaAs-Bi-$AsCl_3$-HCl-H_2-He system were within the interval from 20 to 21 mA/V, their scatter did not exceed 3…5 %. The scatter of device parameters within a single substrate does not correlate with the substrate coordinate in a reactor in the course of growth; it is explained by the heterogeneity of dislocation structure and connected with its electrophysical parameters as well as with various topological effects.

Conclusions

A complex problem has been solved in order to obtain the planar layers of the *i*- n^0-*n*-n^+ type GaAs field-effect transistors with the Schottky barrier in the GaAs-Bi-$AsCl_3$-HCl–H_2-He system. A regime of tin- and bismuth-doped GaAs growth under low-temperature isothermal conditions has been found. Heterogeneity in the thickness less than 3 % and doping level less than 5 % has been achieved. This allowed to improve the GaAs FTSB operating characteristics and achieve the CVC slope values within 20-21 mA/V in one procedure cycle.

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