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Manifestation of the channeling effect when manufacturing JFET transistors

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Abstract. The proposed work covers the tasks of such areas as reducing input currents and bias voltage of integrated operational amplifiers (ICs OA) manufactured according to BiFET technology, the prospect of using JFET transistors in digital circuit technology, Si CMOS technology at 22 nm node and beyond, manufacturing bipolar transistors on ultra-thin layers of the active base and emitter, increasing resistance of ICs to external influences. The main method of experimental investigation of channeling is the construction of impurity distribution profiles using SIMS. In this work to study the channeling effect of boron and phosphorus in silicon was chosen the method for constructing the response surface of the saturation current of JFET for a silicon wafer. The choice of method was based on the high sensitivity of the cut-off voltage and saturation current of the JFET transistor to the channel thickness and impurity concentration in it, the relative simplicity of performance and practical benefits in improving BiFET technology.

Keywords: ion implantation, implanter, channeling, JFET, BiFET.

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1. Introduction

One of the main effects influencing the distribution of impurities introduced using ion implantation is ion channeling – the oriented movement of particles along axial and planar channels. Measurements of range distributions and energy loss in single crystals have revealed directional effects, for slow and heavy ions [1]. The paper [2] describes a theoretical approach to the problems of directional effects for energetic charged particles moving through solids. Planar and axial channeling effects of 3…11 MeV protons in silicon and germanium single crystals were investigated studying the direction and energy distributions of the transmitted particles [3]. The total energy distributions were investigated as a function of crystal orientation using a large-acceptance angle solid-state detector. Limiting angles of incidence for channeling were obtained at several incident energies and crystal thickness values. Measurements of wide-angle (150′) scattering and of ***I*** and ***M*** X-ray yields in tungsten single crystals are reported as a function of crystallographic orientation with respect to an incident beam of 1.4-MeV helium ions [4, 5]. In [6] the effect caused by ion scattering by nuclei was evaluated, and it was found that the scattering angle of the ion beam is significantly smaller as compared to the Si ⟨100⟩ channeling critical angle.

Despite the fact that channeling has been studied since the early 60s [1-7], an adequate analytical model of ion channeling in the low-energy region is still not built and continues to be the subject of theoretical and experimental work.

There are many challenges in semiconductor manufacturing for Si CMOS technology at 22 nm nodes and beyond [8]. The modern process of development in junction technology for advanced scaled devices requires ultra-shallow junction (USJ) with better characteristics, reasonable junction abruptness, and lower junction leakage. However, in the low energy (LE) or ultra-low energy (ULE) regimes, when the device size continues to shrink, there are significant limitations for conventional beam-line (BL)-based ion implants not only on the productivity but also on the device performance, because of fundamental issues like space charge limit, channeling effect, self-sputtering effect, implant angle variation issues, and incurred line of shadowing effect. The channeling effect is most severe for boron-based doping of *p*-type USJ, since boron penetrates much deeper due to a very light ion mass which is easily scattered into the channel.

Axial and planar channeling occurs with low energy losses of the channeling ions. The chains of atoms located in the lattice sites elastically perceive the impulse of a collision as a single whole, transferring it to the neighboring atoms of the chain [9]. The displacement of the chain atom in inelastic collisions with an ion causes a loss of energy and contributes to the dechanneling of ion. Channeling is possible in a narrow range of angles for entry of the beam into the target. The critical angle for channeling is usually greater at low ion beam energies [10]. Experimental studies for phosphorus give a critical dechanneling angle of ≈1° for the family of directions ⟨100⟩ and ⟨111⟩, and ≈2° for ⟨110⟩ (Fig. 1). The capture of an ion with involvement in the movement along the channel can extend over a distance of several thousand periods of the unit cell. For example, for phosphorus at 300 keV, the penetration depth is approximately 1.2 μm, which is four times the depth of the distribution peak with non-canalizing doping.

2. Experience of using ion implantation in the development of IC OA

The use of ion implantation in technology of manufacturing integrated operational amplifier (IC OA) 140UD6 (analogue LM108) for formation of a high-resistance base of the input pair of super-β transistors did not reveal a significant spread across the wafer the value of U_{PT} (punch-through breakdown) of super-β, which strongly depends on the total amount of impurity in the base (dose of $^{11}B \approx 0.5…1$ μC·cm^{-2}, E = 50…100 keV, depth of base x_j is 4.5 μm, base sheet resistivity ρ_{SB} = 5000 Ω/□). The punch-through breakdown is described by the expression:

$$V_{PT} = \frac{q}{2\varepsilon\varepsilon_0}\left(\frac{Q_B^2}{N_C} + Q_B W_B\right), \quad (1)$$

where q is the electron charge, ε – dielectric constant of silicon, ε_0 – vacuum electric constant, N_C – impurity concentration in the collector, W_B – metallurgical width of the base.

Q_B is the total amount of impurity in the base under the emitter per unit area, associated with the resistance of the layer of uniformly alloyed base under the emitter by the relation:

$$Q_B = \frac{1}{q\rho_{SBE}\mu}, \quad (2)$$

where μ is the mobility of the main carriers, ρ_{SBE} – layer resistance of a uniformly doped base under the emitter.

The expression is valid for a uniformly doped base; taking into account the real distribution profile gives insignificant differences from this model [11].

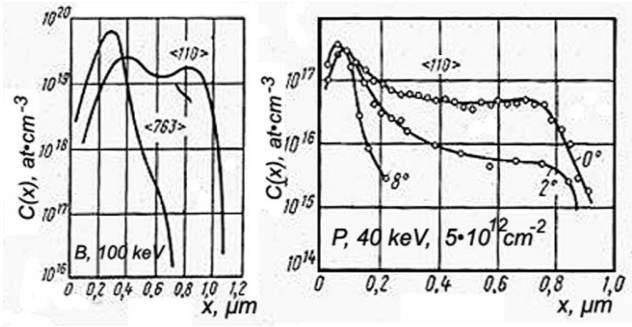


Fig. 1. Channeling of boron and phosphorus in silicon in the direction [110].

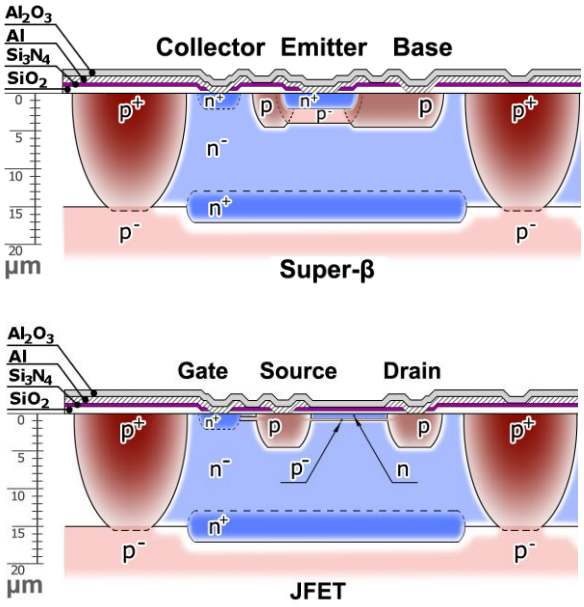


Fig. 2. Cross-section structure of super-β and JFET transistors.

However, the transition to BiFET technology (KR140UD18, analogue LF355) revealed the presence of a significant variation in the cut-off voltage (U_{CO}) of JFET transistors both on the wafer surface and within the same technological batch loaded into the ion-doping process. The cross-section of the structure of super-β and JFET transistors is shown in Fig. 2.

In this case, the order of the dose of ion doping for formation of the upper semiconductor gate (phosphorus) and the JFET channel (boron) is the same as for the high-resistance base of super-β transistors (boron). The total amount of impurity (boron) per unit area for a high-resistance base of a super-β transistor at U punch-through breakdown 1…3 V is (2…4)·10^{11} cm^{-2}, and for a JFET channel at U_{CO} 1 V is (0.8…1.2)·10^{12} cm^{-2}.

The difference is that the shallow layers of the channel and the upper gate of JFET are not subjected to long-term high-temperature distillation, therefore, the impurity distribution obtained in the process of ion implantation is preserved. The cut-off voltage of JFET transistors in BiFET technology is usually within 1 V,

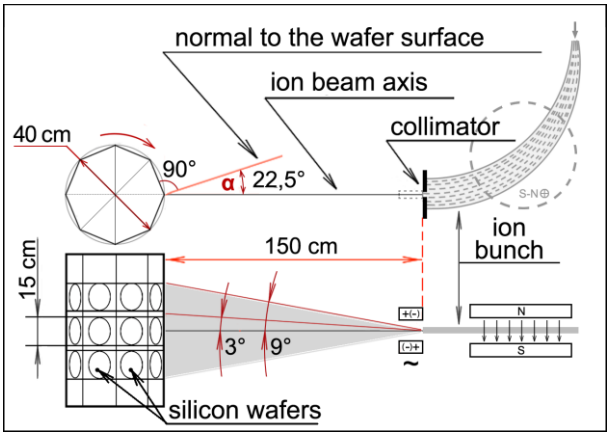


Fig. 3. Scheme of angles of e-beam in the Vesuvius-5 implanter.

the breakdown voltage $U_{GD} \geq 50$ V. This imposes a limit on the thickness of the channel, which should be, respectively, within 1 μm, and on the impurity concentration in the upper gate, which should not exceed 10^{16} cm^{-3}.

$$U_{CO} = \frac{\int_{bot\ p-n}^{top\ p-n} qN_a a^2}{8\varepsilon\varepsilon_0}, \tag{3}$$

$$I_0 = \frac{Wq^2\mu_a N_a a^3}{24L\varepsilon\varepsilon_0} = U_{CO} \cdot a \cdot \frac{W}{L} \cdot \frac{q\mu_a}{3}, \tag{4}$$

where U_{CO} is the cut-off voltage, I_0 – saturation current corresponding to zero voltage at the gate, μ_a – mobility of the main carriers, N_a – impurity concentration in the channel, W – channel width, L – channel length, a – channel thickness.

The cause of the scatter of U_{CO} values in JFET transistors can be the effect of channeling, since the path of ions in channeling is comparable with the thicknesses of the upper gate and the channel. Ion doping was carried out in a Vesuvius-5 implanter, the design of which is shown in Fig. 3.

Placing target wafers on a rotating three-tier octahedral drum with vertical scanning by deflecting the ion beam along the axis of rotation of the drum gives the whole range of doping angles along both axes.

The projection of the ion beam in the doping zone has a diameter of about 2 cm (which corresponds to the theoretical data [9] on the initial divergence of the beam 0.5°). The angle α between the axis of the ion beam and the normal to the surface of the wafer changes as the 8-sided drum rotates from +22.5° at the "advancing" edge of the wafer, passing through 0° in the middle of the wafer, and then the wafer leaves the doping zone under the angle –22.5°. At the same time, different parts of the wafer are under different conditions for channeling. Simulation in Jmol [12] shows that since the drum turns, and the ion beam axis approaches to the perpendicular, several new axial channels become open for a short time. The upper and lower parts of the wafer also differ from the central part by an additional inclination of 3°. On the upper and lower tiers of the drum, the fixed corners of 3° and 9° are added to the lower and upper edges of the wafer, respectively. The real response surface of I_0 (saturation current in JFET at zero voltage U_{GD}) has significant asymmetry due to the fact that the boundaries of the channeling areas for boron (JFET channel) and phosphorus (upper JFET gate) can be misaligned because of the different arrangement of the wafer on the drum in the processes of boron and phosphorus doping, the asymmetry of the drum, and also the scatter of the crystallographic orientation of the initial target wafers (Fig. 4).

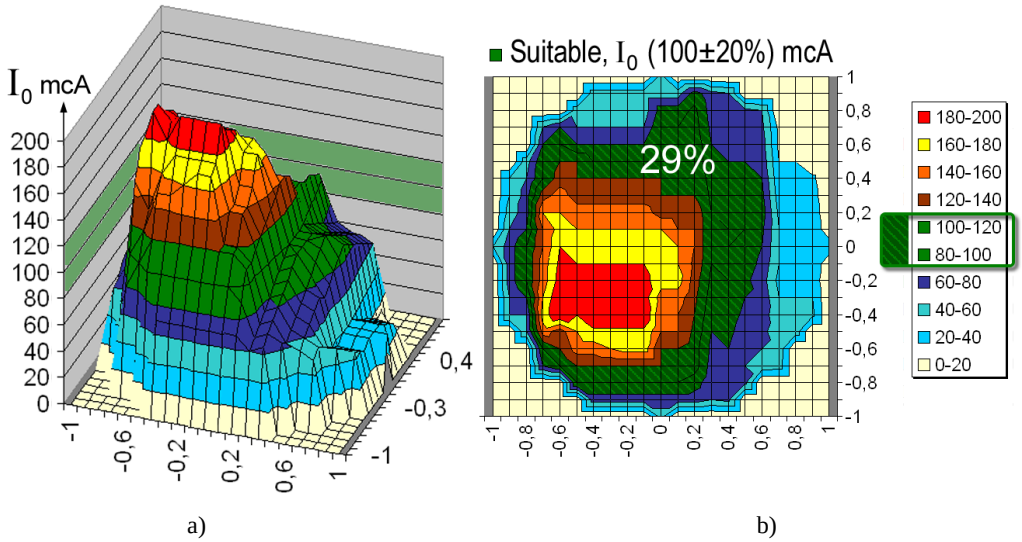
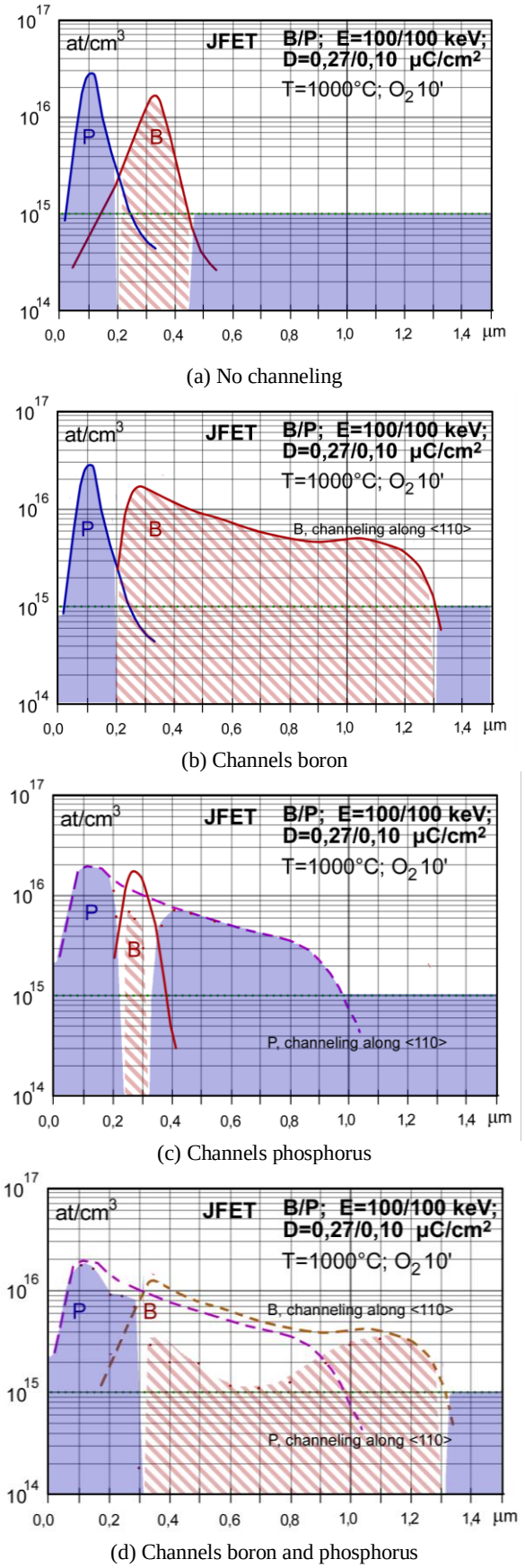


Fig. 4. Real surface response of saturation current JFET (I_0).



(a) No channeling

(b) Channels boron

(c) Channels phosphorus

(d) Channels boron and phosphorus

Fig. 5. Combinations of boron and phosphorus channeling options in the JFET transistor structure.

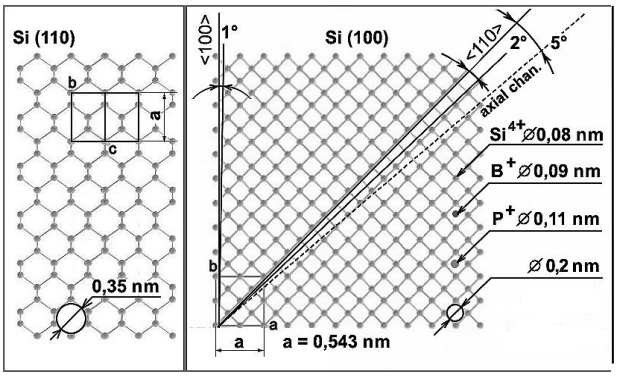


Fig. 6. The projection of the critical angles of channeling ^{11}B and ^{31}P on the crystal lattice of silicon.

3. Discussion

3.1. Combinations of boron and phosphorus channeling

There are four main cases of boron and phosphorus distribution in the channel and the upper gate of the JFET transistor, which can occur at different points on the wafer surface (Fig. 5). The impurity distributions obtained as a result of modeling in the Suprem-3 program are taken as a basis.

The distribution (a) is assumed at the edges of the wafer, (d) – in the center of the wafer, options (b) and (c) – in adjacent areas.

For a differential input pair JFET in the OA scheme, a non-planar response surface according to I_0 and U_{CO} will lead to an increase in the asymmetry of the inputs, which will be reflected by an increase in the offset voltage values. To achieve 100% yield of ICs by using the I_0 parameter, it is necessary to control the doping angle α and dose setting with high accuracy.

3.2. The geometric model of the projection of the critical angles of channeling

The geometric model of the projection of the critical angles of channeling onto the silicon lattice, built in Jmol [12] with account of the known values of diameters of singly charged boron ions (^{11}B) and phosphorus (^{31}P) as well as quadruple charged silicon ions at the lattice sites, gives the values for critical angles the same as in experiment. On the presented projection, the critical angles of channeling fit into the gap between the atomic planes within the five elementary cells of the silicon lattice (Fig. 6).

The goniometric heads for each wafer with adjustable tilt angles in three planes will help to solve this problem. A two-channel ion guide, which allows a testing beam of protons or electrons to be sent to a target, will allow setting the targets with a guaranteed choice of either channeling or its absence, and over the entire surface of the wafer.

3.3. New generation of implanters

Some models of ion implanters are presented in Table.

Table. Ion implanters.

No	Implanter model	Accelerating voltage, kV
1.	Vesuvius 5	100
2.	ILU-5M, Vesuvius 13P	200
3.	K2MV RBS (HVEE), 1989	2000
4.	Singletron & Tandetron* (HVEE)	6000

1, 2 possess the ability to work with ions of a limited set of elements, stepwise control of the result with the adjustment of modes from one process to another.

3. K2MV RBS (HVEE)

- beam energy up to 2 MeV,
- two ion lines (ion implant + structure analysis according to the RBS method),
- goniometric sample head (three degrees of freedom with tuning according RBS method),
- dose irregularities on the wafer less than 1%,
- the spread from a sample to sample does not exceed 2%,
- scanning by moving the target.

4. * Estimated cost of "Singletron" and "Tandetron" models – up to tens million dollars.

4. Conclusions

In the manufacture of ICs using thin diffusion layers obtained by ion implantation, it is necessary to take into account the effect of channeling. To do this, it is necessary to use modern implanters, which allow to accurately fix the angle between the axis of ion beam and crystallographic orientation of the target, as well as providing scanning by moving the target with a fixed ion beam. A mismatch of 1° already creates an unacceptable departure for the cut-off voltage of JFET transistors. One of the wafer placement options is the choice of an "amorphizing" doping angle that completely eliminates channeling. The increasing complexity of equipment and its associated rise in price is inevitable, because there are no other ways to solve this problem. Reducing the cost of an implanter can be achieved by upgrade one of the previous models according to the requirements described above.

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Прояв ефекту каналювання при виготовленні JFET транзисторів

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Анотація. Запропонована робота охоплює завдання таких областей, як зменшення вхідних струмів та напруги зміщення інтегрованих операційних підсилювачів (IC OA), виготовлених за технологією BiFET, перспектива використання транзисторів JFET у технології цифрових схем, технологія Si CMOS на 22-нм рівні і вище, виготовлення біполярних транзисторів на надтонких шарах активної бази та емітера, що збільшує стійкість IMC до зовнішніх впливів. Основним методом експериментального дослідження каналювання є побудова профілів розподілу домішок за допомогою SIMS. У цій роботі для вивчення ефекту каналювання бору та фосфору в кремнії був вибраний метод побудови поверхні відгуку струму насичення JFET для кремнієвої пластини. Вибір методу базувався на високій чутливості напруги відсічки та струму насичення транзистора JFET до товщини каналу та концентрації домішок у ньому, відносній простоті експлуатаційних характеристик та практичних перевагах у вдосконаленні технології BiFET.

Ключові слова: іонна імплантація, імплантер, каналювання, JFET, BiFET.