Semiconductor Physics, Quantum Electronics & Optoelectronics, 2022. V. 25, No 4. P. 379-384.

Semiconductor physics

Scanning probe lithography on Ge(111)-c(2×8) surface

A.M. Goriachko

Taras Shevchenko National University of Kyiv, Faculty of Radiophysics, Electronics and Computer Systems, 4g, Akademika Hlushkova Ave., 03187 Kyiv, Ukraine
E-mail: goriachko@knu.ua

Abstract. The paper describes nanometer scale lithography on atomically clean Ge(111)-c(2×8) surface performed in the ultra-high vacuum scanning tunneling microscope operating at 300 K. Using a standard $Pt_{80}Ir_{20}$ probe tip and applying bias voltages between 0.5 and 3 V, the Ge surface could be reliably imaged with atomic resolution without any modification of the sample. However, surface modification in highly localized area under the probe tip was observed at the bias voltages from 4 to 5 V. Such modification could occur in the form of the deposition of the tip material onto the scanned area of the sample, extraction of the sample material or generation of defects in the sample crystalline structure. Possible physical mechanisms of the processes outlined above as well as the strategies to achieve reliable scanning probe nanolithography are discussed.

Keywords: scanning tunneling microscopy, nanolithography, germanium, platinum, iridium.

https://doi.org/10.15407/spqeo25.04.379
PACS 61.72.uf, 68.35.B-, 68.37.Ef

Manuscript received 16.05.22; revised version received 05.11.22; accepted for publication 14.12.22; published online 22.12.22.

1. Introduction

Nanostructured surfaces are of ever increasing importance for modern science and various high-tech branches like biotechnology, nanoelectronics, nano-catalysis, *etc*. There are two broad classes of techniques capable of creating nanostructures on the surfaces of some suitable substrates: self-assembly [1–3] and nanolithography [4]. Within the context of surface nanostructuring, a self-assembly process essentially attains thermodynamic equilibrium, in which the free energy of the surface is minimized with certain nanostructures being an integral part of it. Such nanostructures can only be investigated and characterized, but their exact size, shape and composition can not be predetermined or predesigned. Contrary to this, in a lithographic process, a structure is created with the geometry, which is preliminary defined or programmed by an engineer.

Ever since its invention, scanning tunneling microscopy (STM) [5] was viewed as a powerful technique for not only observing the atomic structure of surfaces but also for creating nanometer (nm) sized structures (nanostructures) on top of them [6]. The STM based nanolithography is inherently extremely slow, but it is still the only technique capable of assembling nanostructures atom by atom in a predefined manner. This was demonstrated by precise positioning of atoms of noble gasses or metals within the nanostructures formed on top of atomically clean and atomically flat metal substrate in ultra-high vacuum at cryogenic temperatures [7]. In this case, the physical process driving the assembly of atoms into the nanostructure is pushing or pulling an atom adsorbed on the surface by the apex of the STM probe tip. If the tip trajectory can be controlled by the operator, so is the atom's trajectory and its final position. Such nanolithography scheme requires some extra adsorbed atoms to be present on the atomically flat substrate, which can be achieved by evaporating a small amount of material on a specially prepared atomically flat substrate. An alternative process, which can be utilized for atomically controlled creation of nanostructures, is transferring atoms from the tip to the substrate by field evaporation of the tip material [8]. The STM based nanolithography is a slow sequential process. Meanwhile, extremely high throughput parallel nanolithography processes, such as X-ray or extreme ultraviolet lithography [9], already exist providing the best resolution in the nm-range. However, although they are unbeaten in terms of productivity (number of created nanostructures per unit of time), the corresponding equipment is astronomically expensive, difficult to obtain and complicated to operate. Hence, the STM based nanolithography still holds an edge as regards atomic resolution. What is more important, it provides a feasible opportunity to create individual nanostructures with modest investments in the cases, when only few nano-structures are required for scientific research purposes.

Silicon is the mainstream building material for modern integrated electronic circuits. However, other semiconductors are being considered for future generations of nanoelectronic devices. Germanium brings advantage for high frequency devices due to drastically higher carrier mobility as compared to silicon [10]. The Ge(111) surface is of particular interest, because its symmetry matches that of graphene – another important ingredient material in nanoelectronics. It was demonstrated recently that graphene can be grown epitaxially on Ge(111) leading to surface nanostructuring with lateral periodicity of several nm [11]. A whole range of two- and three-dimensional nanostructures were obtained within Bi films adsorbed on Ge(111) as well as zero-dimensional delta-doping centers [12, 13]. Furthermore, the atomically clean Ge(111) surface exhibits certain one- and two-dimensional nanostructuring due to coexistence of the basic c(2×8) and perturbed (2×2) reconstructions [14]. All these recent findings warrant further detailed studies of the Ge(111) surface including the STM based nanolithography proof of concept experiments.

2. Experimental

2.1. Preparation of atomically clean Ge(111) surface

Prior to performing nanolithography on a Ge(111) surface, it should be prepared to make it atomically clean and atomically flat. A sample was cut from a *p*-type (Ga-doped, 0.3 Ohm×cm) Ge wafer with a high quality polished surface. The sample was loaded into an ultra-high vacuum chamber (base pressure 2×10^{-10} mbar), where all experiments were conducted. This chamber was equipped with an electron beam sample heater, an ion gun and a scanning tunneling microscope [15]. Surface preparation consisted of outgassing at 600 K for several hours followed by several cycles of ion bombardment (500 eV Ar^+ ions, ion current density 10 μA/cm^2, 1 minute duration) and annealing (900 K, 1 minute duration). The last step of the surface preparation process was always the annealing at 900 K, but with a gradual cooling to 300 K during 10 minutes. The above described procedure had produced an atomically clean reconstructed Ge(111)-c(2×8) surface consisting of atomically flat terraces separated by monoatomic steps, as confirmed by STM.

2.2. Scanning tunneling microscopy of Ge(111) surface

The scanning tunneling microscope was operated in the constant current mode. The probe tips were made of the Pt80%Ir20% wire (0.25 mm in diameter). The tips were produced by simple cutting with scissors and simultaneous pulling. After loading into the ultra-high vacuum chamber, they were cleaned and sharpened by electron bombardment (electron kinetic energy 2.5 keV, beam current several mA). Scanning was performed in two regimes: imaging and nanolithography, which differ in sample bias voltage. Stable imaging was possible for voltages of both polarities with a magnitude from 0.5 to 3 V and a typical tunneling current of 0.3 nA. Namely, under such conditions, the imaged area of the Ge(111) surface was unaltered on multiple consecutive STM images. The nanolithography regime was also essentially scanning but the sample bias voltage was higher than 3 V. Under such conditions, the arrangement of atoms within the scanned area was changed by the scanning process. This could be confirmed by direct comparing the images obtained under the normal imaging conditions before and after the lithographic scanning.

3. Results and discussion

In the following, an overview of the STM images of the Ge surface before nanostructuring is presented. After that, the exact procedures leading to the surface nanostructuring are outlined and the STM images documenting the resulting surface morphologies are shown.

3.1. STM imaging of Ge(111)-c(2×8) surface

Typical STM images with atomic resolution of the Ge surface obtained by the preparation procedure described in the subsection 2.1 are presented in Fig. 1. They show atomically flat terraces, on which individual atoms of the topmost atomic layer are clearly visible. Fig. 1a shows an area with a single terrace, on which the surface atoms are highly ordered and just a few defects are visible in the field of view. The observed crystalline structure is a well known c(2×8) reconstruction of the atomically clean Ge(111) surface in ultra-high vacuum as described in detail elsewhere (see [14] and the references therein). The area in Fig. 1a contains a single domain with this crystalline structure.

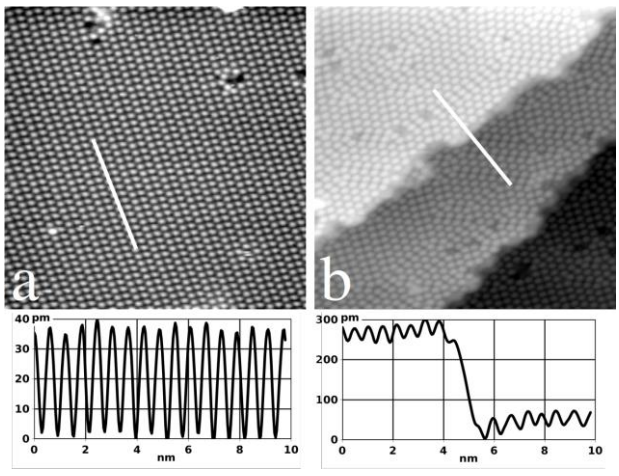

Fig. 1. Empty states STM images (25×25 nm field of view) of the clean Ge(111) surface. The graphs below the images show the height-distance cross-sections obtained along the thick white lines within the field of view. The area with a single atomically flat terrace, the sample bias voltage is +2.5 V, and the cross-section is taken through a single domain (a); the area with three terraces separated by single atomic steps, the sample bias voltage is +1.5 V, and the cross-section is taken across one of the steps (b).

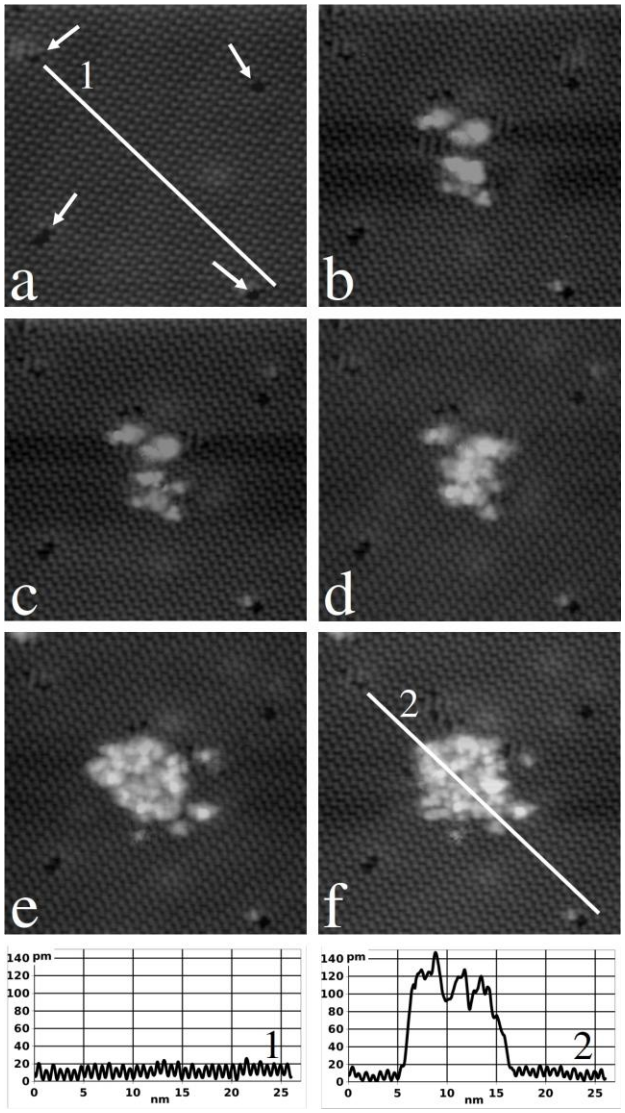

Fig. 2. Empty states STM images (25×25 nm field of view, sample bias voltage +2 V) of the same area on the Ge(111) surface. The images were obtained between the lithographic scanning procedures. Height-distance cross-sections 1 and 2 were taken along the corresponding white thick lines. White arrows point to pre-existing surface defects. Initial state of the surface area (a). Subsequent states of the same surface area after each subsequent lithographic scanning procedure (b–f).

Fig. 1b shows an area, which contains three terraces separated by single atomic steps. Here, a remarkable feature is a high concentration of defects, mostly domain boundaries separating numerous small domains. The height-distance cross-sections taken along the thick white lines withing each corresponding image are shown below the STM images in Fig. 1. These cross-sections allow one to compare the magnitude of the interatomic corrugation within the atomically flat terrace with the height of a single atomic step. To eliminate any uncontrolled influence of pre-existing surface features, all further lithographic procedures are applied only to surface areas of the type shown in Fig. 1a.

3.2. STM nanolithography on Ge(111)-c(2×8) surface

Fig. 2 shows the sequence of steps of our nanolithographic process. Fig. 2a is an STM image of the starting 25×25 nm area in the initial atomically flat state. One may notice four atomic-scale vacancy defects in the crystalline structure of the surface marked by white arrows. They will serve as the "landmarks" enabling unambiguous identification of the area while observing the results of the nanostructuring process. All images in Fig. 2 were obtained at the +2.0 V sample bias voltage, which is typical for the imaging regime of scanning. Each image in Figs 2b–f was obtained after a lithographic scanning procedure, which consisted of scanning a smaller 6×6 nm area in the center of the field of view of Fig. 2 at the sample bias voltage of +4.0 V.

As the STM images in Figs 2b–f clearly demonstrate, such lithographic scanning procedure indeed results in deposition of some material on the sample. Since our probe tip is made of the platinum-iridium alloy, it is reasonable to assume that the observed deposit consists of Pt and Ir atoms in the same proportion as in the tip material (80% Pt, 20% Ir). Moreover, the deposition process is probabilistic in nature, *i.e.* the longer the conditions, which enable field evaporation of atoms from the tip onto the sample, are maintained, the more material is deposited. As expected, the lateral localization of deposition mostly mimics the area where such conditions are created, namely a 6×6 nm square-shaped area in the center of the field of view of the images in Fig. 2. After sufficient number of lithographic scanning procedures, this square-shaped area is completely covered with deposited atoms. The height-distance cross-sections along the lines 1 and 2, being compared to those in Fig. 1, demonstrate that the height of the created nanostructure is of the order of magnitude of a single atomic layer thickness. Therefore, the deposited atoms form the first adsorbed layer on the top of the Ge surface. One may conclude that the described procedure is indeed lithographic, since the lateral pattern of the deposited material is defined by the parameters of this procedure, namely, the shape of the exposed area, which is approximately the square with a side of ~6 nm. It is worth noting that this procedure is not perfect. One can see several atoms deposited outside the targeted square-shaped region, although rather close to its border. The actual size of the created nanostructure is somewhat larger than the intended one, namely ~7×7 nm, meaning that there is a "spill-over" of the atoms during deposition or edge effect. The lateral precision of the described lithographic procedure can thus be estimated at roughly 1 nm. An additional side effect of the lithographic scanning is generation of defects in the crystalline structure of the Ge surface. Such defects, which are not present in the initial state of the surface, can also be seen outside the patterned square, but within the field of view in Fig. 2. Finally, the metal atoms are non-ordered and numerous irregularities are visible within the created nanostructure. These effects can also be formally considered as the imperfections of our lithographic procedure.

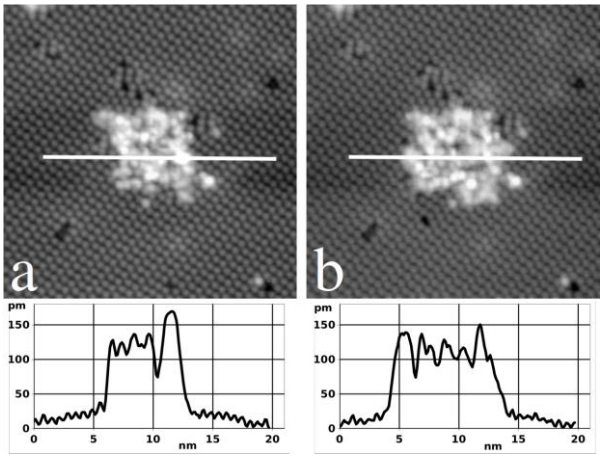

Fig. 3. Empty states STM images (25×25 nm field of view, sample bias voltage +2 V) of the same surface area as in Fig. 2 after continuing the lithographic scanning procedure at the unchanged parameters (a, b).

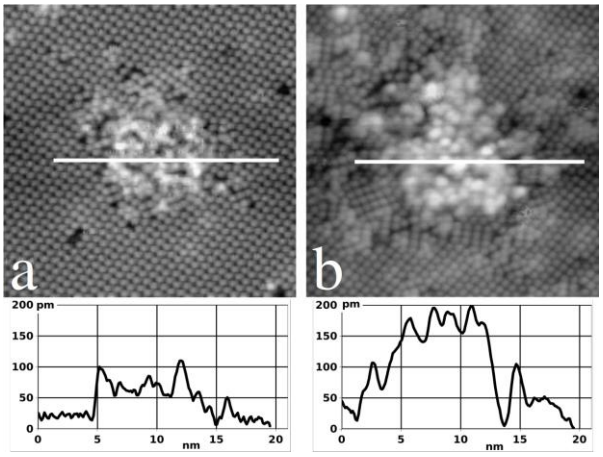

Fig. 4. Empty states STM images (25×25 nm field of view, sample bias voltage +2 V) of the same surface area as in Figs 2 and 3 after continuing the lithographic scanning procedure at the +4.5 V sample bias voltage (a) and at the +5 V sample bias voltage (b).

Fig. 2 demonstrates the laterally controlled deposition of the first atomic layer of metallic adsorbates on the Ge substrate. A natural question then arises: Can we deposit the second and subsequent layers by continuing the process? Unfortunately, this turns out not to be the case. Fig. 3 presents the results of additional lithographic scanning steps at the parameters identical to those employed for the sequence in Fig. 2. As the height-distance cross-sections taken along the white thick lines in Figs 3a and 3b clearly show, no second atomic layer of the metallic adsorbate is formed on the top of the existing square-shaped island. Instead, some additional material is deposited onto the Ge substrate outside the targeted 6×6 nm square region due to a spill-over effect. This can be noticed by carefully comparing Figs 2f with 3a and 3b. Furthermore, there are visible changes within the targeted 6×6 nm square region indicating that despite the absence of additional deposition, the lithogrpahic scanning procedure providing the structures presented in Figs 3a and 3b causes rearrangement of previously deposited atoms.

It appears from the data of Fig. 3 that no lithographically useful deposition of the tip material takes place at +4 V bias voltage if one atomic layer has already been deposited in the given location. Such outcome may be because of the redistribution of the local electric field due to the presence of a metal island on the semiconductor surface. A natural conclusion is that the resulting field is not sufficiently high to cause field evaporation of atoms from the tip. Therefore, the sequence of the lithographic scanning procedures on the same 6×6 nm square region as in Figs 2 and 3 was continued at increased sample bias voltage. Lithographic scanning of the given surface area in the state depicted by Fig. 3b was performed at +4.5 V sample bias voltage, after which the STM image in Fig. 4a was obtained. Thereafter, one more lithographic scanning was performed at +5 V, after which the STM image in Fig. 4b was obtained.

Fig. 4a shows a somewhat unexpected result, namely, instead of depositing additional material onto the substrate, some already deposited material is removed. This is clear from direct comparison of cross-sections in Figs 3b and 4a showing less material adsorbed on the Ge surface after the lithographic scanning procedure at +4.5 V than before. It is reasonable to conclude that field evaporation of atoms from the sample onto the tip takes place in this case. At even higher sample bias voltage of the lithographic scanning procedure, namely +5 V, field evaporation of the tip material onto the sample is achieved again, as can be seen from the STM image in Fig. 4b and the corresponding cross-section. However, it is also obvious that the quality of the lithographic process has deteriorated rather significantly. The lateral shape of the deposit no longer resembles the targeted 6×6 nm square. There is a very strong spill-over effect and intensive defect generation over the entire 25×25 nm surface patch corresponding to the field of view in Fig. 4b. One may say that the lithographic scanning procedure at the + 5 V sample bias voltage is no longer atomically precise as expected from the STM technique.

The obtained results presented in Figs 1–4 may be qualitatively explained by field evaporation of atoms from both the tip and the sample surfaces. However, this process is facilitated by inelastic tunneling current, which is always present in STM experiments and amounts to roughly several percent of the total tunneling current [16]. Due to the inelastic tunneling, the energy is spent on atom vibrations around their equilibrium positions, which is known to be an essential step of the field evaporation process. This is equally true for the atoms in both the tip and the sample. Therefore, both of them can undergo field evaporation, thus opening the way for bidirectional material transfer between the tip and the sample. However, creating a meaningful lithographic pattern must imply transferring matter exclusively in one direction: either depositing the tip material onto the sample or extracting the sample material. The results of

Figs. 1–4 suggest a practical recipe to achieve this, namely by increasing the bias voltage in the smallest possible steps until the transfer becomes detectable. Since the atoms at the apex of the STM probe tip are lower coordinated than on the flat surface, the threshold for their evaporation should be lower than for the atoms the flat surface consists of.

The side effect of the vibrational excitations by inelastic tunneling current is formation of defects within the substrate. The defects are formed because the energy is transferred from the tunneling electrons to the atoms located in certain vicinity of the smallest tip-to-sample gap. This side effect is clearly undesirable as it modifies the surface outside the lithographically scanned area, thus effectively blurring the borders of the created nanostructure. Here too, the strategy to minimize the defect generation within the crystalline structure of the substrate is to perform lithographic scanning at the smallest possible bias voltage. This strategy is applicable if the defects themselves are not the intended constituents of the created nanoscale pattern.

Lower absolute value of the bias voltage during the lithographic scanning is also desirable for reducing the spillover effect or deposition of atoms outside the targeted lithographic pattern. Once an atom is field evaporated from the tip apex as an ion, it is accelerated toward the sample. Higher absolute value of the voltage between the tip and the sample means higher kinetic energy once the ion reaches the sample. After neutralization the atom moves around until this energy is dissipated and can come to rest away from the landing position. Therefore, smaller absolute bias voltages and thus smaller kinetic energies help to reduce the time of full energy dissipation and lead to smaller distance covered by an atom on the surface.

One aspect of the presented lithographic prospect still remains unclear. Namely, there is no simple qualitative explanation of why the deposition saturates when one atomic layer of platinum-iridium mixture is present on the surface (Fig. 2f). This can only be understood based on *ab-initio* calculations of electronic structure and tunneling current combined with molecular dynamic simulations of atomic ensembles in the vicinity of the tunneling junction.

In conclusion, this paper demonstrates a successful nanolithography using the STM technique in a particular case of nanometer-precise deposition of a mixture of Pt and Ir atoms on the top of atomically clean Ge(111)-c(2×8) surface.

Acknowledgements

All data were processed using an open-source Gwyddion software, which can be downloaded for free at http://gwyddion.net/ [17]. This work was supported by the Ministry of Education and Science of Ukraine (Grant No. 21БП052-02).

References

1. Goriachko A., Over H. Modern nanotemplates based on graphene and single layer h-BN. *Z. Phys. Chem.* 2009. **223**. P. 157–168. https://doi.org/10.1524.zpch.2009.6030.
2. Goriachko A., He Y., Knapp M. *et al*. Self-assembly of a hexagonal boron nitride nanomesh on Ru(0001). *Langmuir*. 2007. **23**. P. 2928–2931. https://doi.org/10.1021/la062990t.
3. Afanasieva T.V., Fedorus A.G., Goriachko A.M. *et al*. Mesoscopic self-ordering in oxygen doped Ce films adsorbed on Mo(112). *Surf. Sci*. 2021. **705**. P. 121766. https://doi.org/10.1016/j.susc.2020.121766.
4. Rani E., Wong L.S. High-resolution scanning probe nanolithography of 2D materials: Novel nanostructures. *Adv. Mater. Technol.* 2019. **4**. P. 1900181. https://doi.org/10.1002/admt.201900181.
5. Bian K., Gerber C., Heinrich A.J. *et al*. Scanning probe microscopy. *Nat. Rev. Methods Primers*. 2021. **1**. Art. No 36. https://doi.org/10.1038/s43586-021-00033-2.
6. Voigtländer B., Cherepanov V., Korte S. *et al.* Multi-tip scanning tunneling microscopy: Experimental techniques and data analysis. *Rev. Sci. Instr*. 2018. **89**. P. 101101. https://doi.org/10.1063/1.5042346.
7. Khajetoorians A.A., Wegner D., Otte A.F., Swart I. Creating designer quantum states of matter atom-by-atom. *Nat. Rev. Phys*. 2019. **1**. P. 703–715. https://doi.org/10.1038/s42254-019-0108-5.
8. Katnagallu S., Dagan M., Parviainen S. *et al*. Impact of local electrostatic field rearrangement on field ionization. *J. Phys. D: Appl. Phys.* 2018. **51**. P. 105601. https://doi.org/10.1088/1361-6463/aaaba6.
9. Maldonado J.R., Peckerar M. X-ray lithography: Some history, current status and future prospects. *Microelectron. Eng*. 2016. **161**. P. 87–93. https://doi.org/10.1016/j.mee.2016.03.052.
10. Scappucci G., Kloeffel C., Zwanenburg F.A. *et al*. The germanium quantum information route. *Nat. Rev. Mater.* 2021. **6**. P. 926–943. https://doi.org/10.1038/s41578-020-00262-z.
11. Goriachko A., Melnik P.V., Nakhodkin M.G. A suggestion of the graphene/Ge(111) structure based on ultra-high vacuum scanning tunneling microscopy investigation. *Ukr. J. Phys.* 2016. **61**. P. 75–87. https://doi.org/10.15407/ujpe61.01.0075.
12. Goriachko A., Melnik P.V., Shchyrba A. *et al.* Initial stages of Bi/Ge(111) interface formation: A detailed STM study. *Surf. Sci*. 2011. **605**. P. 1771–1777. https://doi.org/10.1016/j.susc.2011.06.004.
13. Goriachko A., Shchyrba A., Melnik P.V., Nakhodkin M.G. Bismuth growth on Ge(111): evolution of morphological changes from nano-crystals to films. *Ukr. J. Phys.* 2014. **59**. P. 805–818. https://doi.org/10.15407/ujpe59.08.0805.
14. Goriachko A., Melnik P.V., Nakhodkin M.G. New features of the Ge(111) surface with co-existing c(2×8) and 2×2 reconstructions investigated by

scanning tunneling microscopy. *Ukr. J. Phys*. 2015. **60**. P. 1132–1142.
https://doi.org/10.15407/ujpe60.11.1132.

15. Lyubinetsky I.V. Key role of M.G. Nakhodkin's insight and inspiration in development of UHV STM-related techniques and methods. *Ukr. J. Phys*. 2015. **60**. P. 160–164.
https://doi.org/10.15407/ujpe60.02.0160.
16. Minamitani E., Takagi N., Arafune R. *et al*. Inelastic electron tunneling spectroscopy by STM of phonons at solid surfaces and interfaces. *Prog. Surf. Sci*. 2018. **93**. P. 131–145.
https://doi.org/10.1016/j.progsurf.2018.09.002.
17. Nečas D., Klapetek P. Gwyddion: an open-source software for SPM data analysis. *Centr. Eur. J. Phys*. 2012. **10**. P. 181–188.
https://doi.org/10.2478/s11534-011-0096-2.

Author and CV

Andrii M. Goriachko, Doctor of Sciences in Physics and Mathematics, Associate Professor of the Faculty of Radiophysics, Electronics and Computer Systems at the Taras Shevchenko National University of Kyiv. He is the author of more than 70 scientific publications. His research interests include physics of nanostructured surfaces and 2D materials, scanning probe microscopy, electron spectroscopy and diffraction.
https://orcid.org/0000-0003-2963-5010

Сканувальна зондова літографія на поверхні Ge(111)-c(2×8)

А.М. Горячко

Анотація. У статті описується літографія в нанометровому масштабі на атомарно чистій поверхні Ge(111)-c(2×8), виконана в надвисоковакуумному сканувальному тунельному мікроскопі, що працює при 300 K. З використанням стандартного вістря $Pt_{80}Ir_{20}$ і застосуванням напруги зміщення між 0,5 і 3 В за абсолютною величиною, поверхня германію може бути досліджена з атомною роздільною здатністю без будь-яких модифікацій зразка. Однак під напругою зміщення від 4 до 5 В за абсолютною величиною відбувалася дуже локалізована модифікація поверхні під вершиною вістря. Така модифікація може відбуватися у формі осадження матеріалу вістря на сканованій ділянці зразка або вилучення матеріалу зразка, або утворення дефектів у кристалічній структурі зразка. Обговорюються можливі фізичні механізми вищеописаних процесів, а також стратегії досягнення надійної сканувальної зондової нанолітографії.

Ключові слова: сканувальна тунельна мікроскопія, германій, платина, іридій, нанолітографія.