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An arithmetic logic unit of a computer based on single electron transport system

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Abstract. A simple two-way switching can be modified utilizing optical switching, electron-wave modulation and single-electron transport. In this work an arithmetic-logic unit is designed by employing single-electron Binary Decision Diagram devices (or circuits). The design is done for a single bit of the arithmetic-logic unit. The total design will be obtained by cascading desired number of such bit stages.

Keywords: binary decision diagram, buffer, electron injector, electron transport.

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1. Introduction

Civilization of mankind advances step by step. It has been conferred incalculable benefit from technological world. Now civilized mankind is at the door of more advanced technology. The more he (mankind) is getting advances, the more his responsibility for invention increases. The tremendous desire for invention makes him to face the challenges in the competitive world of technology. In microelectronics, one of the challenges is to develop LSI's based on a new paradigm for digital processing. For doing so, we must first look for or create a device which can perform the logic operation in such a way totally different from the way they are performed by ordinary transistors[1-3]. An approach to such new devices can be built on the basis of the concept of binary decision diagrams (BDDs)[4,5]. The unit function of this device is a simple two-way switching. A binary decision diagram represents a digital function as a directed cyclic graph with each node labeled by a variable. It provides a complete and concise representation for most digital functions encountered in logic-design applications. For convenience, single electron transport has been utilized in this present BDDs by which a more complicated and sophisticated combinational circuit representation (such as ALU) can be implemented [6,7]. Noted that, it should even be possible for a BDD device to use a single electron as a messenger, and there are several single-electron-tunneling structure [8-10]that could be used to make such a device. This device is the key element in LSI's based on single electron devices.

A digital module such as arithmetic logic unit (ALU) can be implemented with the help of these BDDs. Buffers are also used for appropriate time maintenance for the operation of ALU. The principle operation of the ALU resides under the control of the carriers (specially electrons) passing through all BDDs processed by the signal input potentials. The principle of coulomb blockade of single electron tunneling is followed by this device (ALU as well as BDD). As ALU based on single electron BDD device is inexpensive, consumes less power and operates with least time, this device can best be exploited for scientific, business, educational and security purposes. Technologists get spirited and their hopes and inspirations grow exponentially for the merits of BDD devices. For the survival of the fittest, this single electron technology is going to revolutionize the manufacturing process and production. With a new structure and new phenomenon, this technology leads to open a new horizon in the electronics devices / circuits / equipments. So, we are optimis-

tic, in near future that the triumphs of this technology of microelectronics of LSI's on the basis of single electron BDDs will precede exponentially.

2. Design of an ALU

Arithmetic logic unit can be designed with the help of the several binary decision diagram devices, each representing separate Boolean function. The output of each BDD device is connected to some other appropriate BDD device for getting required Boolean function. The arithmetic section is designed in such a way that it is independent of logic section. Then the so designed arithmetic unit is checked for realization of logic functions without any modification of the desired arithmetic unit. The circuit is then modified in such a way that it can perform all logical operations but such modifications should not disturb the realization of arithmetic functions. So, we should design the arithmetic section first. We would like to use four selection signals (which is sufficient for realization of all arithmetic logical operations) such as S_2, S_1, S_0 and C_{in} and two input combinations A_i and B_i. As there are four selection signals, there are $2^4 = 16$ combinations. If we put $S_2 = 0$ then we have $2^3 = 8$ inputs which can be selected by S_1, S_0 and C_{in}. i.e. we get eight arithmetic outputs as depicted in the Table 1.

Table 1.

Selection S_2	S_1	S_0	C_{in}	Output (F_i)	Function
0	0	0	0	A_i	Transfer
0	0	0	1	$A_i + 1$	Increment
0	0	1	0	$A_i + B_i$	Addition
0	0	1	1	$A_i + B_i + 1$	Add with carry
0	1	0	0	$A_i - B_i - 1$	Subtract with borrow
0	1	0	1	A_i – Bi	Subtraction
0	1	1	0	$A_i - 1$	Decrement
0	1	1	1	A_i	Transfer

These operations can be implemented using single electron BDD circuits, which consist of the four cycles of seven phases each. During each cycle specific operations are performed. Results of each intermediate operations are depicted in the various locations of Fig. 1. Finally, any of the desired eight functions is available at F_i output depending on the selection variables. A complete arithmetic circuit for performing all those eight arithmetic operations is shown in Fig. 1.

In the Fig. 1

$$X_i = A_i \tag{1}$$

$$Y_i = S_0 B_i + S_1 \overline{B}_i \tag{2}$$

$$Z_i = C_{in} \tag{3}$$

$$F_i = A_i + S_0 B_i + S_1 \overline{B}_i + C_{in} \tag{4}$$

The arithmetic circuit is now to be modified in such a way that it can perform logical operations. However, the modification should not restrict the realization those of eight arithmetic operations.

We pay heed to the logic section. Without affecting the operations of arithmetic section we can choose $S_2 = 1$, $C_{in} = 0$ so there are only two selection lines S1 and So. And there are only $2^2 = 4$ combinations fit to be selected. It is understood that all logical function can be realized with the help of three primary logic gates i.e. AND, OR and NOT. As there are two selection variables (S_1 and S_0) so $2^2 = 4$ logical input combination can be utilized. The additional logic function which can be incorporated is XOR function as it helps to realize many combinational functions directly. The logical operation table is shown in Table 2.

Table 2.

S_2	S_1	S_0	X_i	Y_i	C_{in}	F_i	Operation Required	Obtained Operation
1	0	0	A_i	0	0	A_i	Transfer	OR
1	0	1	A_i	B_i	0	$A_i \Sigma B_i$	XOR	XOR
1	1	0	A_i	$\overline{B}_i$	0	$A_i \odot B_i$	Equivalence	AND
1	1	1	A_i	1	0	$\overline{A}_i$	NOT	NOT

In Table 2 when $S_2S_1S_0 = 1\,0\,0$, the output function $F_i = A_i$. Hence, A_i is to be replaced by $A_i + S_2 \overline{S}_1\ \overline{S}_0 B_i$ to get required logical operation which is OR function in the present case. In the third row of the same table it is seen that $F_i = A_i \odot B_i$. But it's expected value is $A_i B_i$. So, A_i is to be replaced by $A_i + S_2 S_1 \overline{S}_0\ \overline{B}_i$. By combining the above two conditions the final A_i will be

$$A_i + S_2 \overline{S}_1\ \overline{S}_0 B_i + S_2 S_1 \overline{S}_0\ \overline{B}_i . \tag{5}$$

Thus the final arithmetic logic unit is represented in Fig. 2 which requires four cycles and seven phases in each cycle to complete an operation (either arithmetic or logic operation). In the Fig. 2

$$X_i = A_i + S_2 \overline{S}_1\ \overline{S}_0 B_i + + S_2 S_1 \overline{S}_0\ \overline{B}_i \tag{6}$$

$$Y_i = S_0 B_i + S_1 \overline{B}_i \tag{7}$$

$$Z_i = \overline{S}_2\, C_{in} \tag{8}$$

Thus here we designed ALU. For the regular pattern of this unit, we can increase the unit number by cascading the identical single units according to the bit size of the ALU.

3. Explanation

The entire system (ALU) is composed of the BDD tree circuits, electron injectors, buffers and output interfaces. The circuit designed for the ALU is depicted in Fig. 2. In each circuit, a root node is indicated by Root, terminal nodes are indicated by buffers.

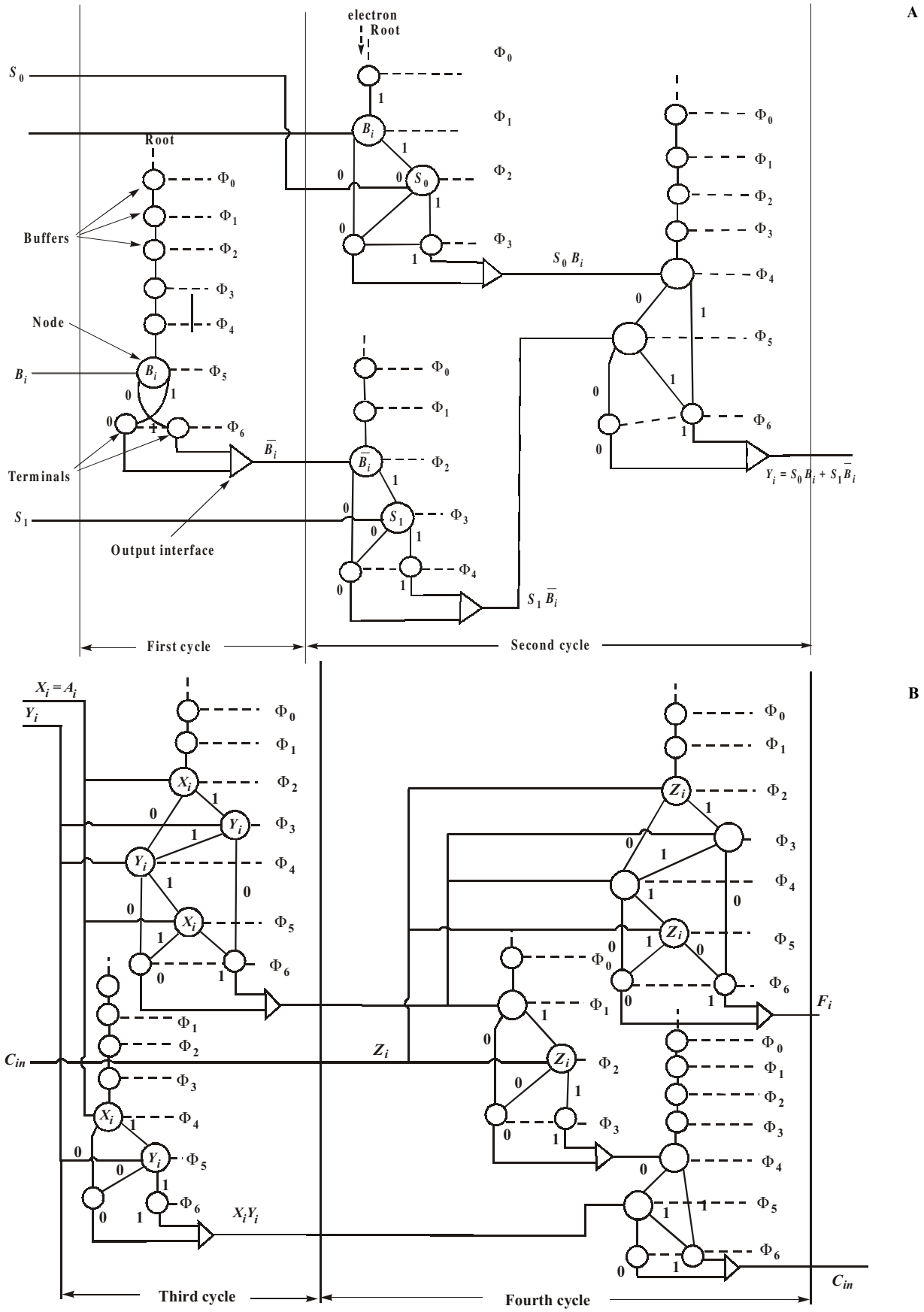

Fig. 1. Single electron BDD circuit of an arithmetic unit for single bit consisting of four cycles of seven phases each. Each cycle is shown separately (Fig. 1A represents first and second cycles of operation and Fig. 1B represents third and fourth cycles of operation).

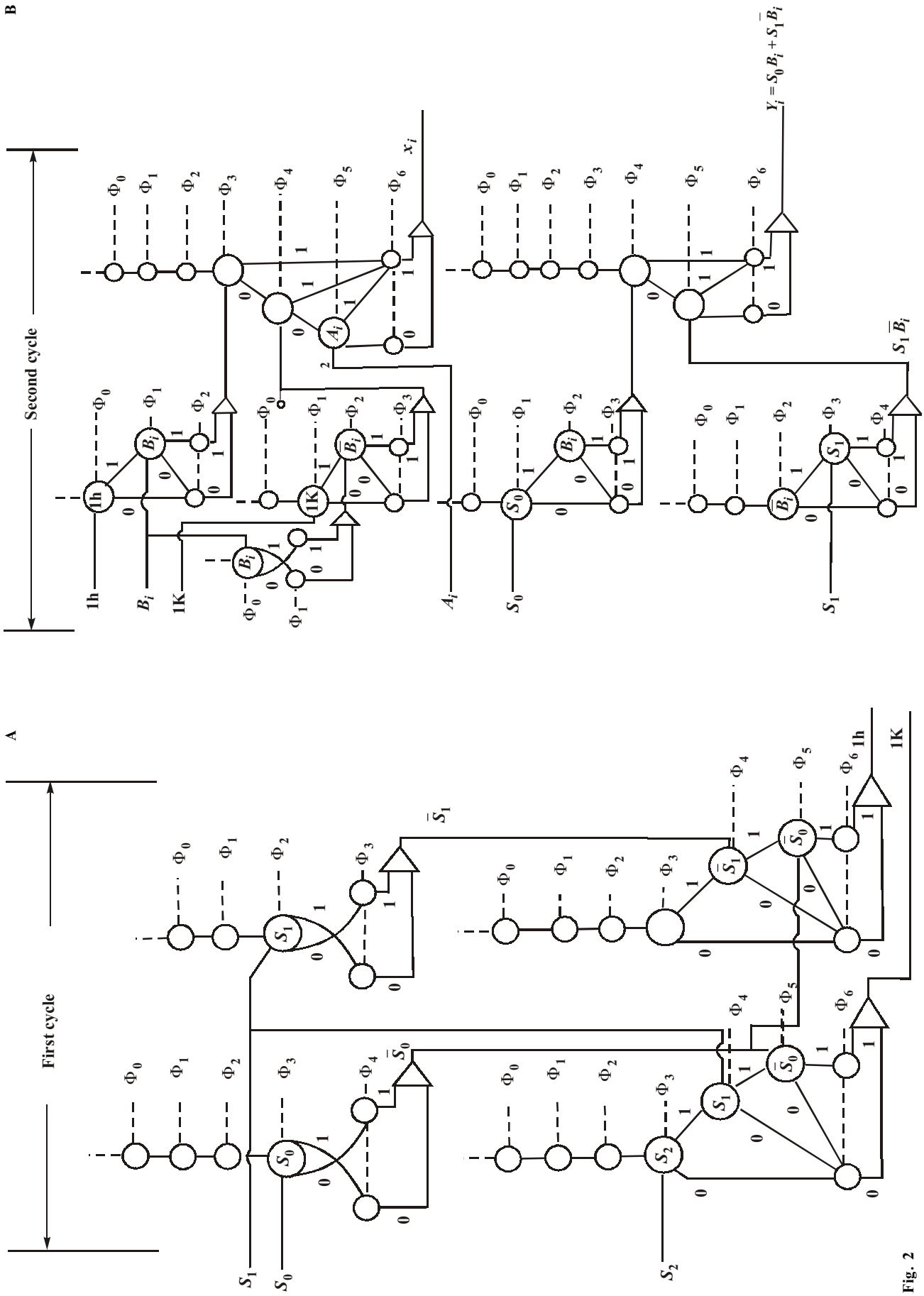
B
A
Second cycle
First cycle
1h
1K
B_i
A_i
S_0
S_1
S_2
x_i
$Y_i = S_0 B_i + S_1 \bar{B}_i$
$S_1 \bar{B}_i$
$\bar{S}_0$
$\bar{S}_1$
Φ_0 Φ_1 Φ_2 Φ_3 Φ_4 Φ_5 Φ_6

Fig. 2

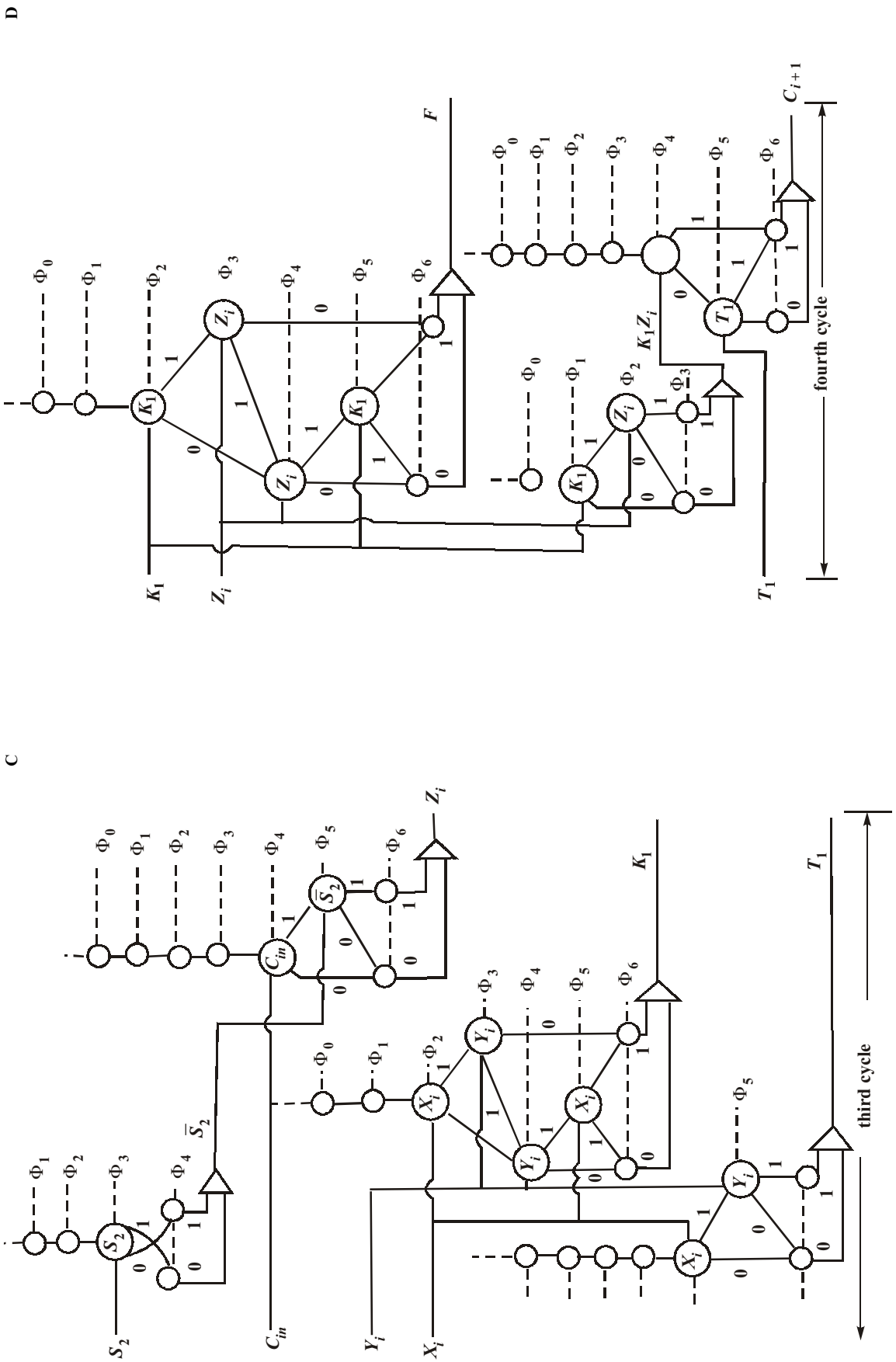

Fig. 2. Single electron BDD circuit of an arithmetic logic unit for single bit consisting of four cycles of seven phases each. Each cycle is shown separately (Fig. 2A, Fig. 2B, Fig. 2C and Fig. 2D represent first, second, third and fourth cycle of operations, respectively].

To transfer the messenger electron in the circuit, seven-phases (Φ_0 through Φ_6) clock is applied to nodes and buffers. The phase-shift of the clock are $\Phi_0 = 0$, $\Phi_1 = 2\pi/7$, $\Phi_2 = 4\pi/7$, $\Phi_3 = 6\pi/7$, $\Phi_4 = 8\pi/7$, $\Phi_5 = 10\pi/7$, $\Phi_6 = = 12\pi/7$. Hence, the desired result is available at the output of the ALU after four clock cycles. The bit signals of the circuit inputs are applied in sequence to the nodes such that the bit signal for a BDD device is applied synchronously with the clock pulse for the consecutive BDD device (or the consecutive buffers).

For successful operation in such a situation, buffers must be set up on the appropriate points on the path to ensure that a messenger electron will reach at BDD device (or will exit from BDD circuit) at the correct time. Only one electron has been used in a BDD circuit at one clock cycle, so pipelined operation is necessary here.

In Fig. 2 only one stage has been drawn but the diagram can easily be extended in a cascading manner for desired number of bits characterizing the ALU.

4. Conclusion

We have proposed a method to design a arithmetic logic unit based on single electron logic systems using Binary Decision Diagram. Necessary and most related requirements for the design are elaborately discussed. Performance of the designed circuit is tested for some elementary arithmetic and logic operations. The operation error caused by thermal agitation is not included in our design.

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