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Active layer – semi-insulating substrate interface effect on GaAs MESFET components

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Abstract. This paper describes the polarization effect of the substrate on the electric characteristics of the GaAs Metal Semiconductor Field Effect Transistor (GaAs MESFET). An analysis based on the existence of a double space charge at the interface active layer – semi-insulating substrate is applied to determine the active layer and interface parameters. The properties of the drain current and the output admittance characteristics as well as the physical phenomena inherent to this interface are assigned to the dynamic response of the double space charge region.

Keywords: GaAs MESFET, active layer, semi-insulating substrate.

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1. Introduction

The active layer – semi-insulating substrate interface properties influence on the GaAs MESFET electrical and hyper frequencies characteristics.

Gallium arsenide is material possessing numerous traps and defects, which are difficult to be controlled. Indeed, the active layer can be affected close to the interface by the presence of many crystallographic defects that contribute to decrease the free carrier's mobility in this area. Substrate imperfections are also responsible for presence of the interfacial barrier between the substrate and active layer. In order to study the properties of this interface, an experimental observation of different phenomena caused by the interface was performed in our work.

The work comprises the following researches of gallium arsenide semi-insulating substrate (1) and the active layer – semi-insulating substrate interface properties (2).

2. Experimental underlining of different phenomena inherent to the interface

The gallium arsenide Schottky gate field effect transistor structure comprises a semi-insulating chrome compensated substrate on which a heavily doped gallium arsenide epitaxial layer was grown (Fig. 1). A layer deposited on the *n*-layer consists of the gate electrode with the rectangular shape; an ohmic contact called as the substrate electrode may be realized by alloying on

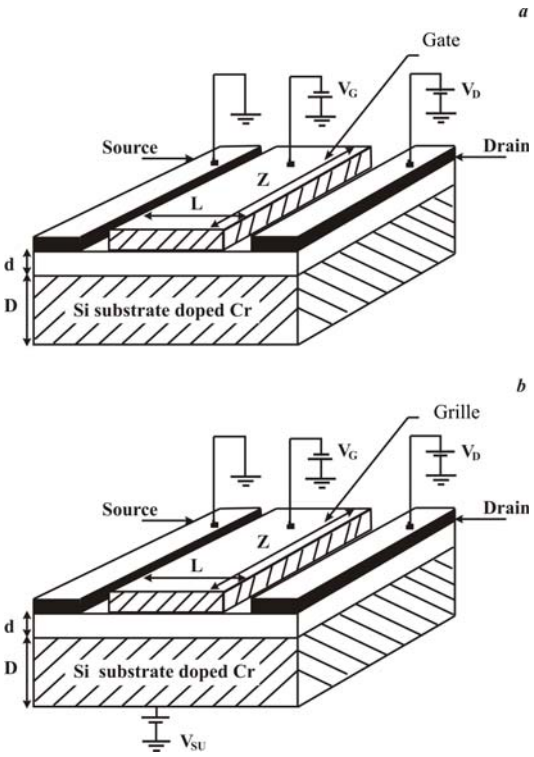

Fig. 1. GaAs MESFET structure without (a) and with (b) substrate polarization.

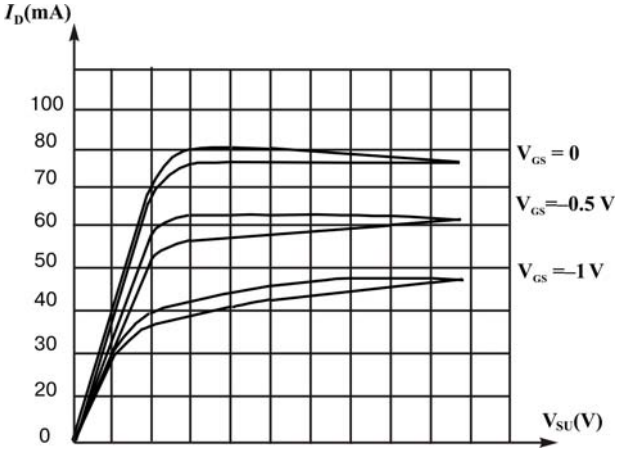

Fig. 2. Characteristics network $I_{DS} = f(V_{DS})$, for $V_{GS} = 0$, –0.5 V, –1 V, presenting an hysterisis phenomenon.

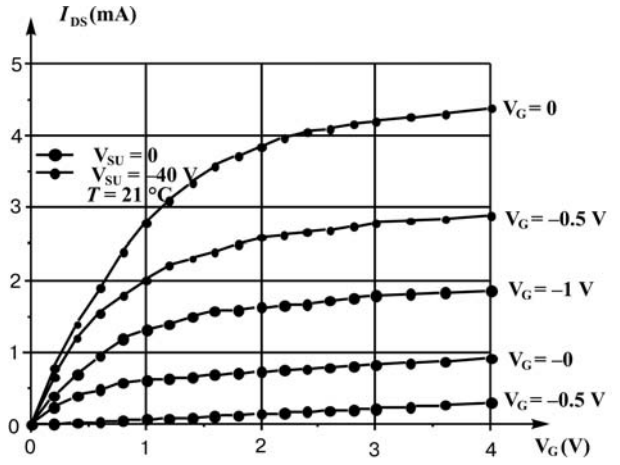

Fig. 3. Substrate effect, I_D (V_{DS}, V_{GS}) as a function of the substrate voltage.

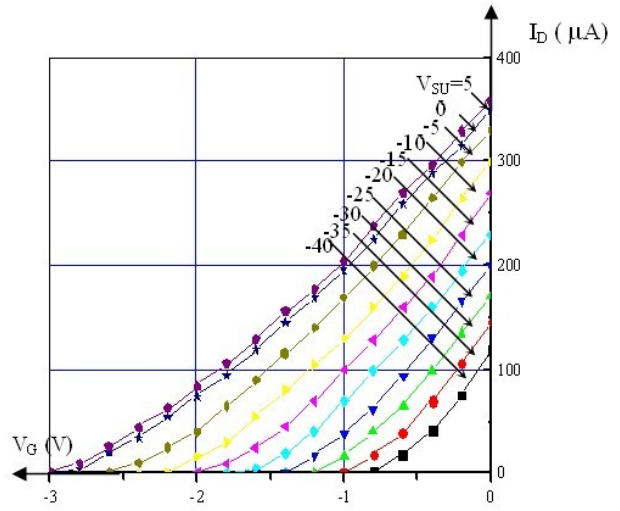

Fig. 4. Transfer characteristics as a function of the substrate voltage.

the back face of the semi-insulating substrate. The active layer – semi-insulating substrate interface characteristics significantly influence on the MESFET GaAs electrical and hyper frequency properties.

The substrate imperfections are responsible for the interfacial barrier presence between the substrate and active layer. For this reason, the GaAs MESFET quality is often worsened by several parasite effects that perturbate its operation.

To begin studying these interface properties, we first present an experimental underlining of various phenomena observed at this interface.

2.1. Hysteresis and bend effects on the output static characteristics network

These hysteresis and bend effects occur as anomalies in the I_D (V_{DS}, V_{GS}) characteristics of some GaAs MESFETs. In a saturation mode (Fig. 2), it has been observed by several authors and attributed to the interface epitaxial layer – semi-insulating substrate traps. These phenomena induce an essencial deterioration of GaAs MESFET hyper frequency performances.

3. Substrate polarization influence

3.1. On the output characteristics

In Fig. 3, we presented the I_D (V_{DS}, V_{GS}) output characteristics parameters as a function of the substrate voltage. We noticed a drain current decrease when a negative voltage is applied to the substrate (Fig. 4).

3.2. On the transfer characteristics at low polarization level

In Fig. 5, we carried out the drain current (I_D) variations as a function of the gate voltage (V_{GS}) at weak drain voltage (V_{DS}) and for several substrate voltages. The characteristic is translated along the vertical axis.

3.3. On the threshold voltage V_T

The threshold voltage represents the gate voltage for which the extension of the carriers depleted space charge is performed in all the semiconductor material. For this particular gate voltage value, the drain current cancels. In our case, Fig. 5 represents the experimental determination of this voltage from the I_D (V_G) characteristic in the ohmic region at very weak V_D. Some authors use the I_D (V_G) variations in the saturation region, the obtained V_T value being different from that obtained in the ohmic region. In the case where a polarization voltage is applied to the substrate, from the previous characteristics, we have carried out the threshold voltage variations with the substrate polarization (Fig. 6). In this figure, we can see three distinct regions as a function of the substrate voltage value: first, the decreasing region, then the saturation

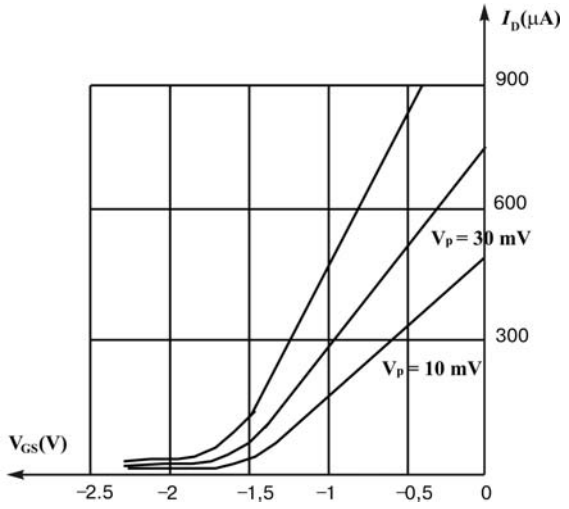

Fig. 5. Variations of the drain current I_D as a function of the Gate voltage at weak drain-source voltage, determination of the threshold voltage V_T.

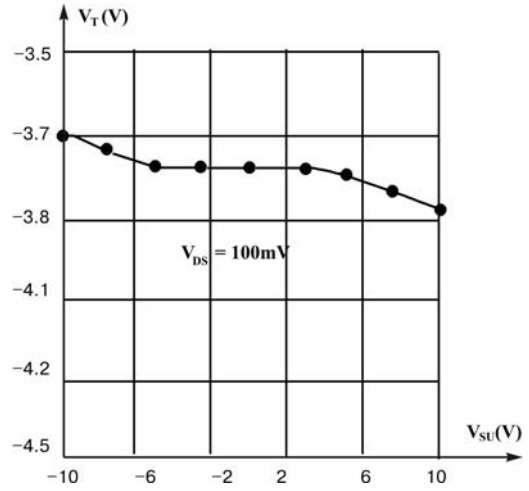

Fig. 6. Variation of the threshold voltage as function of the substrate polarization.

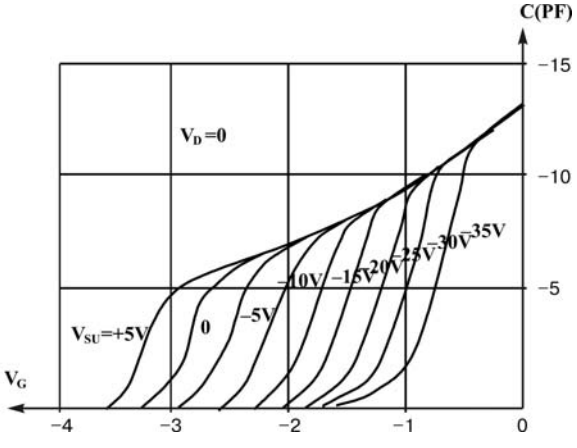

Fig. 7. Experimental variations of the inverse gate capacity as function of the gate voltage for different substrate voltage values V_{SU}.

one, and finally a slope down for the positive substrate voltages.

3.4. *On the input capacity dispersion*

In Fig. 7, the gate dynamic capacity versus the gate voltage for different substrate voltage values is shown. Three different regions in the characteristics are distinguished: a slow variation, a sudden drop, and a region where the capacity tends toward a null value. The first region corresponds to an inverse polarized Schottky diode capacity.

Then the capacity is associated to the residual electronic charge modulation in the space charge zone when the threshold voltage is reached. The negative values of the substrate voltage causes a translation of the characteristics while the positive values have a slight influence.

Regarding the fact that this characteristic depends on the substrate polarization, the question arises again of the methods for the profile doping determination from the $C(V)$ curves.

3.5. On the output conductance dispersion

When the drain voltage varies according to a sinusoidal law in the time, the drain current characteristic as a function of voltages depends on the frequency value. To study this frequency dependence, we carried out the output conductance variations in small signals of these structures.

In the Nyquist diagram, the imaginary part variations as a function of the real part are in a half circle, parameter as a function of the frequency (Fig. 8). This circle exists whatever the operating regime, in the ohmic region or in the saturation region. This conductance dispersion leads to an essential deterioration of GaAs MESFET hyper frequency performances and particularly the power gain.

4. Phenomena interpretation

Some authors interpreted the GaAs MESFET operating anomalies by a trapping mechanism that occurs at the active layer – substrate interface. For our part, we explain these different phenomena by the presence of a double space charge at the interface. Indeed, when we apply a positive drain voltage whether a voltage is applied or not to the semi-insulating substrate, a potential partition occurs between the active layer and the semi-insulating substrate which gives space charge regions in the structure:

1. A space charge region under the gate with a width (W) due to the reverse gate-source polarization (Fig. 9).
2. A superficial fixed charge that exists at the semiconductor – semi-insulating interface is analogous to that found in the semiconductor – insulating structures.

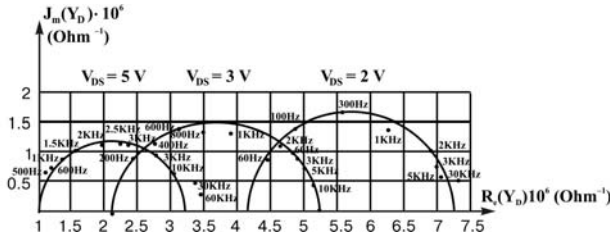

Fig. 8. Evolution in the low frequency of the output impedance of the GaAs.

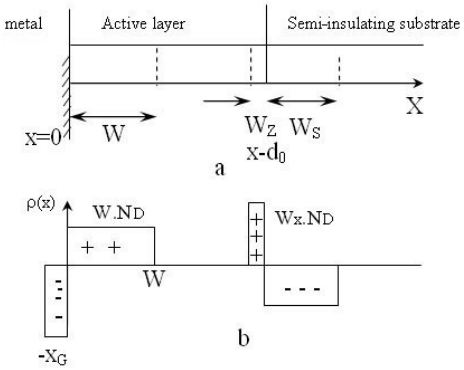

Fig. 9. Double space charge: a – space charge in the GaAs MESFET, b – charge density.

3. Space charges of different parts of the interface to satisfy the electrical induction continuity law with widths W_Z and W_S.

A positive space charge in the semiconductor is due to ionized impurities (N_D), and a negative space charge in the semi-insulating substrate is due to impurities that make the substrate semi-insulating.

5. Conclusion

The GaAs MESFET operation anomalies are interpreted by the presence of a double space charge at the interface, which is liable to be modulated by a polarization variation of the substrate; it produces a channel thickness modulation, and consequently a drain current reduction occur. This explains the experimental variations of the output characteristics when the substrate is polarized.

These physical phenomena are attributed to the interface deep traps that not only influence on the GaAs MESFET performances but also essentially limit integrated circuits based on GaAs MESFET components.

So the origin of hysteresis relaxation mechanisms and bend effects is caused by the double space charge developed at the interface. The output conductance modification is due to response of deep centers. These phenomena lead to transient instabilities of commutation circuits based on GaAs MESFET.

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